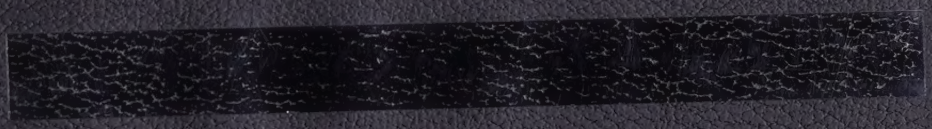

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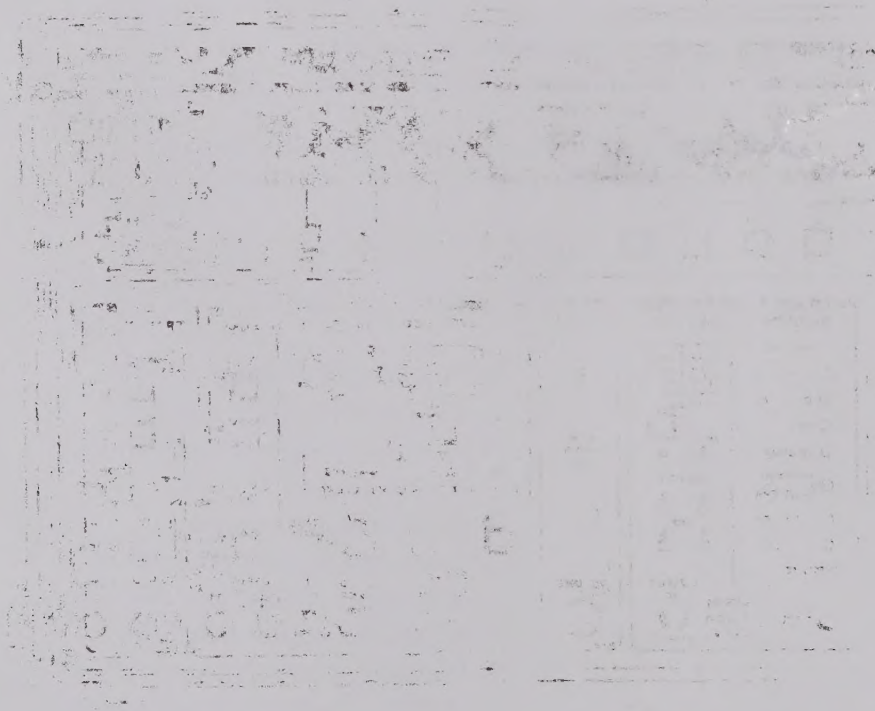

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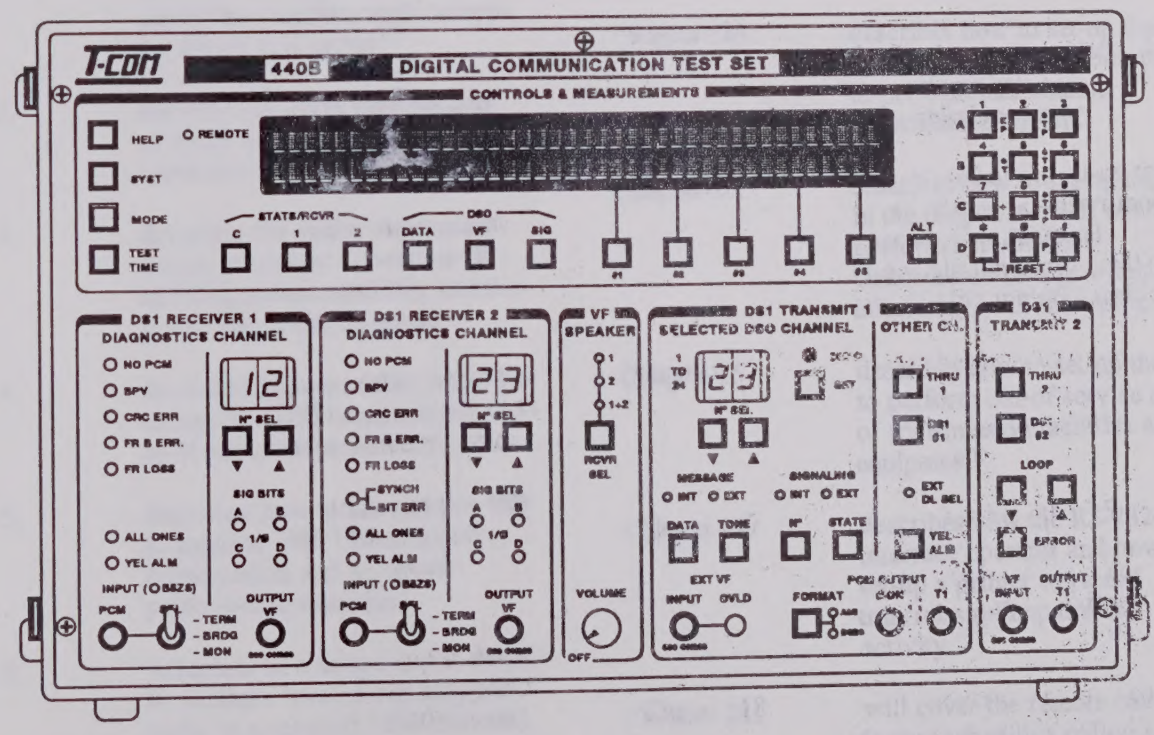
MODEL 440B

INSTRUCTION MANUAL

DIGITAL COMMUNICATION TEST SET



Instrument S/N : 440B 0438

HW/SW Release : 04/04

Instruction manual No. : IM440B-01

Date Issued : October 1990

Chapter 10. describes how to set-up the 4105 to send data in a DSO channel.

Chapter 12. describes how to set-up the 4105 to send information in a DSO channel.

Chapter 13. describes how to set-up the 4105 to derive information in a DSO channel.

Chapter 14. describes how to set-up the 4105 to perform half-duplex transmission testing.

Chapter 15. describes how to set-up the 4105 to perform half-duplex transmission testing without affecting live traffic.

Chapter 16. describes how to set-up the 4105 to perform in-service testing of transmission facility equipment.

Chapter 17. describes how to set-up the 4105 interface operators and how to set-up a printer to receive transmission information.

Chapter 18. will describe how to control features which are available.

ABOUT THIS MANUAL ....

If you have never used the 440B and you would like to become thoroughly familiar with the capabilities and the operation of this instrument, we recommend that you spend some time reading this manual. The reading of the first 3 chapters in particular, is highly recommended. From there on, you may just want to study the chapters of immediate interest. To derive the most benefit from the reading, we suggest that you set-up the instrument nearby and exercise it as indicated in the text.

For ease of reading and reference, the material in this manual has been organized in 25 chapters. A brief overview of the content of each chapter follows.

Chapter 1. provides a fairly comprehensive overview of the 440B capabilities and the applications for which it is suited.

Chapter 2. describes in-depth the function of every key, led, jack, connector and what have you.

Chapter 3. describes the initial instrument set-up procedure as well as the self-diagnostic capability and the system-level keys/menus.

Chapter 4. describes how to set-up the 440B to monitor DS1 transmission and to obtain performance statistics.

Chapter 5. describes how to set-up the 440B to monitor DS0 Channel data transmission and to obtain performance statistics.

Chapter 6. describes how to set-up the 440B to measure level, frequency and noise in a selected DS0 channel.

Chapter 7. describes how to set-up the 440B to display the signaling states and measure wink parameters.

Chapter 8. describes how to set-up the 440B to capture and display MF/DTMF or DP encoded Telephone No.'s.

Chapter 9. describes the use and the application of the loudspeaker.

Chapter 10. describes how to set-up the 440B to send data in a DS0 channel.

Chapter 11. describes how to set-up the 440B to send VF/tones in a DS0 channel.

Chapter 12. describes how to set-up the 440B to send supervision in a DS0 channel.

Chapter 13. describes how to set-up the 440B to send telephone numbers in a DS0 channel.

Chapter 14. describes how to set-up the 440B in the terminal emulation mode to perform half-channel transmission testing.

Chapter 15. describes how to set-up the 440B in the drop-and-insert mode to perform half-channel transmission testing without interfering with the traffic.

Chapter 16. describes how to set-up the 440B to perform out-of-service testing of transmission facilities and equipment.

Chapter 17. describes how the RS-232-C interface operates and how to set-up a printer to record transmission impairment activity.

Chapter 18. will cover the remote control feature when this option is available.

Chapter 19. describes how to use the auxiliary access ports located on the 440B rear panel.

Chapter 20. describes how to unpack, inspect, install the 440B and how to add new options.

Chapter 21.	contains the 440B specifications.
Chapter 22.	describes the self-testing procedures.
Chapter 23.	provides a set of field calibration procedures.
Chapter 24.	contains a list of accessories and replaceable parts available from T-COM for the 440B.
Chapter 25.	contains warranty related information.

Note :
This instruction manual describes the operation of the 440B equipped with all the options except for options 52B and 53A which are covered in separate instruction manuals. Appropriate notations are made in the text to identify the option-specific features.

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1. 440B CAPABILITIES OVERVIEW

INTRODUCTION

1.1 The 440B is an extremely versatile instrument. It has been designed to address a wide range of test requirements related to PCM based communication systems and transmission. In brief, the 440B can be used for qualifying almost any new digital communication system and to maintain it over its operational life.

It is the purpose of this chapter to help the reader develop a degree of familiarity with the 440B capabilities. To this end, this chapter is divided in three sections :

- Basic instrument capabilities
- 440B optional capabilities
- Applications overview

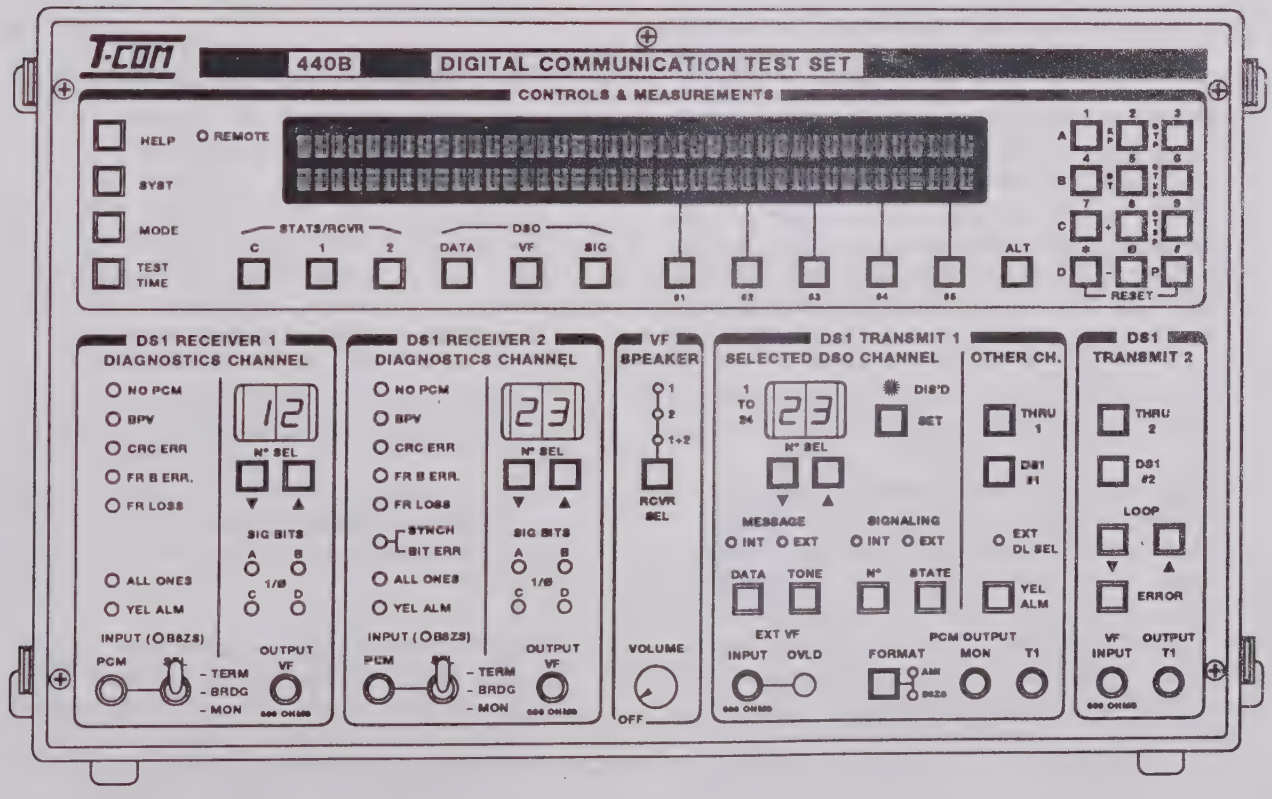


Figure 1-1. The 440B Front Panel

BASIC INSTRUMENT CAPABILITIES

1.2 The 440B, in essence, consists of a set of two DS1 receivers, two DS1 transmitters and a powerful measurement data processor.

These subsystems can operate either independently of each other to perform simple tests, or in concert to perform relatively more complex ones. Each of these subsystems is conveniently confined to a dedicated section of the front panel as illustrated by the front panel line drawing in figure 1.1.

The two DS1 receivers are nearly identical. They differ only in that the second receiver can display bit errors and pattern synchronization when performing out-of-service tests if option 05 is installed. The capabilities common to both receivers include :

- real-time display of PCM transmission impairments
- real-time display of PCM messages
- DS0 channel drop with VF signal and signaling state decoding

The two DS1 transmitters are quite different from one another. The Transmit 1 is dedicated to in-service testing. All patterns delivered by this transmitter are channelized and conform to the DS1 format. The transmitter offers considerable flexibility in the selection of the content of a selected DS0 channel. The selected channel can contain either

- data generated internally
- data supplied from an external source (with option 03)
- discrete tones supplied from a built-in synthesizer
- VF signals supplied by an external source
- signaling generated internally
- signaling supplied by an external source
- MF, DTMF or DP encoded telephone numbers generated internally (only when option 06 is installed)

The Transmit 2, on the other hand, primarily delivers patterns used in out-of-service testing. In particular, this transmitter can generate any number of loop patterns as well as a number of stress patterns such as 3/24, 1/8 and QRS. It can, however, also supply DS1 formatted streams as is required to perform drop and insert testing.

The measurement data processor collects and processes the DS1 transmission data and DS0 data delivered by the two DS1 receivers. Upon user request, the processed data is displayed by the vacuum fluorescent display tube (VFDT) in a readily usable form. The measurements capabilities provided by the basic instrument include:

- in-service transmission statistics for receiver 1 and 2
- DS0 data display and analysis
- VF level and noise measurements
- signaling state display for all 24 channels simultaneously

440B OPTIONAL CAPABILITIES

1.3

- **Option 03** provides an interface to data test sets such as the KS 20908 and KS20909 made by AT&T Technologies or the TPI 108 and TPI 109 made by Telepath Inc. This interface enables analysis of the data contained in a DS0 channel selected from the bit streams monitored by either DS1 receiver. Alternatively, this interface enables the sending of an externally supplied 64 kb/s data stream into a selected DS0 channel in the DS1 stream delivered by the Transmit 1.

- **Option 04** provides an RS-232-C interface port suitable for connecting a printer or a modem to the 440B. When a printer is connected either locally to the 440B or via a modem, one can obtain a record of the time and date stamped impairment activity captured and processed by the data measurement processor.

- **Option 05** provides two sets of capabilities: DS1 out-of-service testing and DS0 data send/receive.

  The DS1 out-of-service testing capability includes the sending and the analysis of a family of stress patterns. These patterns include : 3/24, 1/8, 2^{15}-1, 2^{20}-1 with 14 consecutive zero limitation, 2^{23}-1 and a 24-bit user-defined word. All these patterns may be framed or unframed. The analysis yields the number of bit errors, the number of seconds during which synchronization is lost and the average bit error rate over the duration of the test.

  The DS0 data send/receive capability allows the 440B to deliver and analyze a family of test patterns. These patterns include : 511, 2047 and an 8-bit user-defined byte. The analysis

yields the number of bit errors, the number of block errors, the number of seconds during which synchronization is lost and the average bit error rate over the duration of the test.

- **Option 06** provides for the sending and the recovery of MF, DTMF and DP encoded telephone numbers. In addition, when the 440B is equipped with this option, it can perform single or multiple wink measurements. Up to 16 test telephone numbers can be stored in memory and sent upon demand. Each number, regardless of the encoding type can have up to 32 digits or characters.

- **Option 07** provides for the operation of the 440B under remote control. At the time of this writing, this feature is still being defined; consequently operating details are not yet available.

- **Option 52B** extends the capabilities of the 440B to the DS3 rate. When the 440B is equipped with this add-on unit, a single DS0 channel can be monitored and analyzed from the 672 DS0 channels carried by the monitored DS3 stream. The 52B also displays in real-time transmission impairment events detected at both the DS3 and the DS2 rates. The processed data are available to the 440B and can be printed in the same manner as the data processed by the 440B.

- **Option 53A** extends the capabilities of the 440B to the DS1C rate. When the 440B is equipped with this add-on unit, a single DS0 channel can be monitored and analyzed from the 48 DS0 channels carried by the monitored DS1C stream. The 53A also provides the display in real-time of all transmission impairment events detected at the DS1C rate. The 440B collects and processes the DS1C impairment data and the results can be displayed and printed in the same manner as for the DS1 impairments.

> **Note**
>
> A 440B may be equipped with either option 52B or 53A. All options can be combined as required. These options can be installed in the field with just a few hand tools. Installation instructions are found in chapter 21.

APPLICATIONS OVERVIEW

1.4 The 440B is designed to be used in the central office or the communication center to qualify newly installed digital communication systems and to help the craft personnel maintain and troubleshoot the equipment. The application field can thus be divided into out-of-service testing applications and in-service testing applications.

OUT-OF-SERVICE TESTING APPLICATIONS

1.4.1 The two main applications areas are: PCM transmission facility testing and equipment functional check or acceptance testing.

PCM transmission facility testing requires all the capabilities of the 440B when it is equipped with option 05. This allows the user not only to loop a line, but to send a variety of test patterns to stress the facility and to perform simultaneously a comprehensive real-time transmission performance evaluation.

The 440B can also be used to test a variety of DS1/T1 based equipment to either ensure their conformity with the specifications or to validate their functionality prior to placement into service. Typically, the 440B is then configured to act as a channel bank, both sending PCM test signals and monitoring and analyzing the bit stream delivered by the equipment under test. Specifically, the applications of the 440B in this mode include the testing of all DS1 and DS0 transmission parameters for PCM channel banks, multiplexers (M1C and M13), transmultiplexers, echo cancellers etc.

IN-SERVICE TESTING APPLICATIONS

1.4.2 This 440B is particularly well suited to perform non-disruptive transmission performance testing. To this end, the 440B can be configured to perform:

- passive monitoring of one or two DS1/T1 circuits
- simplex or full duplex-drop-and insert
- single DS0 channel loop back

In all these modes, the 440B can analyze the content of a single DS0 channel whether it contains VF, signaling (MF/DTMF/DP encoded), supervision or data.

The bulk of this instruction manual provides detailed information on all the areas touched in this chapter.

Happy reading.

2. FAMILIARIZATION WITH THE 440B FEATURES

INTRODUCTION

2.1 As may readily be observed from an review of the front panel illustrated in figure 2.1, the user interface is in appearance quite complex. A maze of keys, switches and LED's make this front panel forbidding indeed. But do not let the appearance discourage you, for in reality, you will most likely find that for all its capabilities, this is the easiest set you have ever used.

To accomplish this objective, the front panel combines a number of single purpose hardware features such as keys and LED's with a number of software based menus. In this chapter, we will cover the functions of every front panel key and LED's and, in the process, also review to a limited extent some of the software based features. We will also cover all the rear panel hardware features. A detailed coverage of the software based features is provided in chapters *3* through *15*.

FRONT PANEL FEATURES

2.2 In the description below, the numbers match the circled numbers in figure 2.1.

DS1 RECEIVER #1 AND #2

2.2.1 The two Receiver sections are nearly identical and, as a consequence, the features are described only once.

1 **NO PCM** -- This LED flashes for 50 ms when a string having more than 15 consecutive 'zero' bits is detected. It lights continuously when the PCM bit stream amplitude is not compatible with the input configuration requirements or when the monitored line is oscillating.

2 **BPV** -- This LED flashes for 50 ms when two consecutive 'one' bits having the same polarity are detected. If the line carries B8ZS, only the illegitimate bipolar violations are displayed.

3 **CRC ERR** -- This LED flashes for 50 ms when a CRC-6 discrepancy is detected, indicating that one or more bits were in error during the transmission of the previous 24 frames. This LED is operational only when the D5-ESF mode is selected.

4 **FR BIT ERR** -- This LED flashes for 50 ms when the state of a framing bit (FT) is in error. This LED is operational only when FR LOSS LED is not lit.

5 **FR LOSS** -- This LED lights when framing is not acquired or has been lost. Framing loss occurs when two out of five frame bits are in error.

6 **ALL ONES** -- This LED lights when the monitored PCM bit stream consists of an uninterrupted sequence of unframed "one" bits during at least 50 ms. A framed all-ones sequence does not cause this LED to light.

7 **YEL ALARM** -- This LED lights when the remote (yellow) alarm code is detected. For SLC-96, D1D, D2, D3/D4/D5 this alarm code requires that bit two in each channel is set to zero state for at least 50 ms. For D5-ESF this alarm code requires that the data link message consist of a minimum of 14 consecutive sequences of 8 'ones' followed by 8 'zero' bits.

8 **B8ZS** -- This LED lights when the B8ZS code is detected on PCM input bit stream, independently of the system selection.

9 **CHANNEL No** -- This two-digit LED display shows the selected DS0 channel number being monitored. Any one of the 24 channels may be chosen.

10 **CHANNEL SEL** -- Each depression of the UP or DOWN keys changes the monitored channel number by one in the selected direction. Roll-over occurs between channels 1 and 24 when changes are made continuously in one direction. If a key is held depressed for over one second, the number selected change at the rate of 3 counts per second.

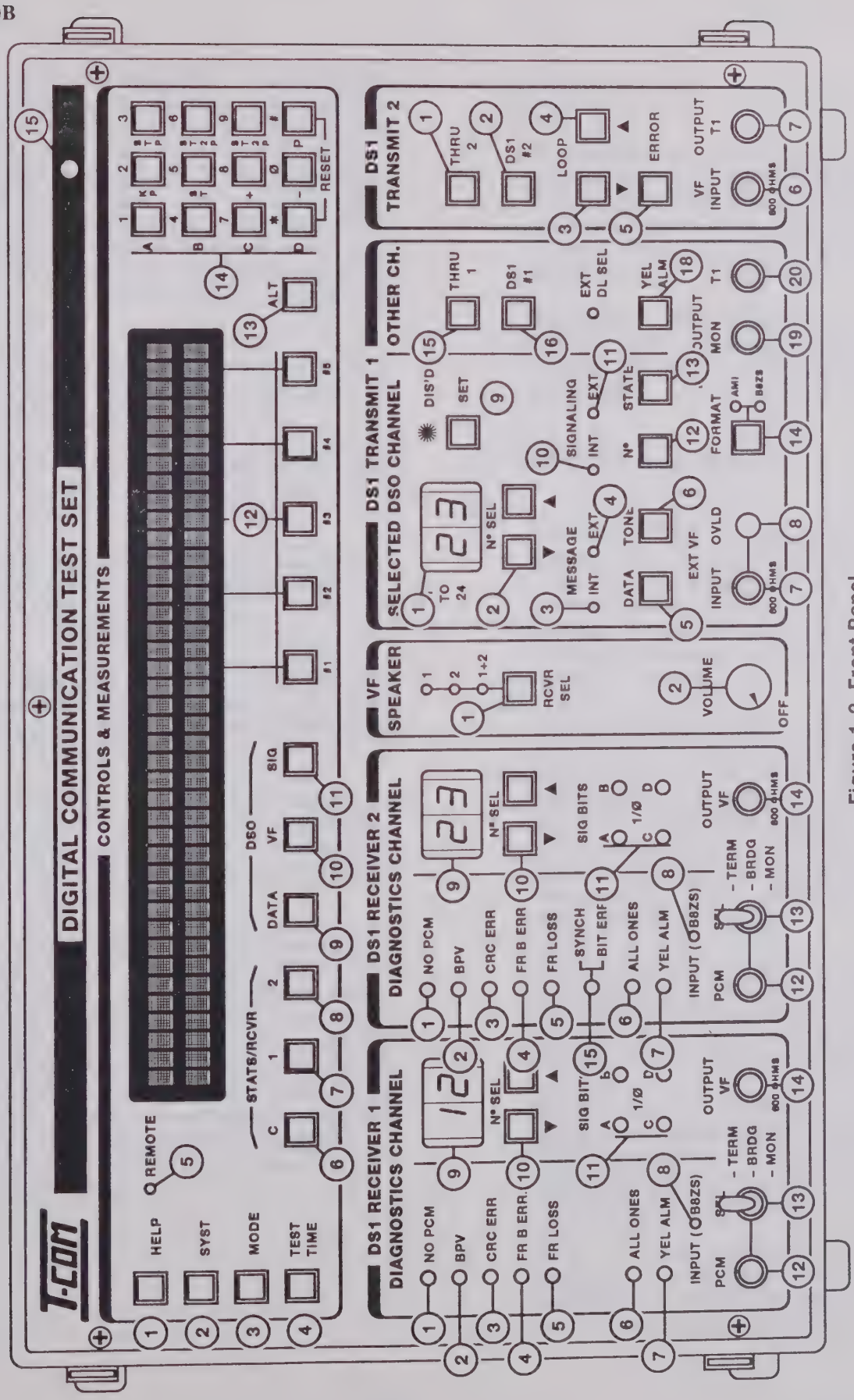


Figure 1-2. Front Panel

11 **A-B-C-D (Signaling bits)** -- These 4 bi-color LEDs display the signaling states associated with the DS0 selected channel. A red colored light corresponds to state "1"; the green colored light to state "0". Signaling bits C and D light only when the ESF format selection prevails. When the FR LOSS (frame loss) LED is lit, the signaling bits are turned off. For Receiver #2, the signaling bits are also turned off when pattern synchronization prevails.

12 **INPUT - PCM** -- This jack receives the PCM bit stream to be monitored and analyzed by the Receiver section.

13 **INPUT - SEL** -- This toggle switch selects the circuit conditions from these three choices:

TERM (100 ohms termination/DSX level)
BRDG (1000 ohms bridging/DSX level)
MON (100 ohms monitoring/
-20 dB DSX level)

The handle of this safety switch prevents accidental movement by locking into groves at its base. To change the setting, the handle must be pulled out.

14 **OUTPUT - VF** -- This jack accesses the decoded VF content of the selected channel. The level on this output is normalized such that 0 dBm = 0 dBm0, when a 600-ohm load or termination is provided.

15 **SYNCH/BIT ERROR** -- This bi-color LED is operational only when option 05 is installed in the 440B. When pattern synchronization is obtained, the green colored light shines. When pattern synchronization prevails and a bit error is detected, the green light turns to red during 50 ms. Pattern synchronization is obtained only when the monitored bit stream is identical to the DS1 pattern selected in the Transmit 2 section.

VF SPEAKER SECTION

2.2.2

1 **RCVR SEL** -- The depression of this switch changes the selection of the DS1 Receiver from which the DS0 channel VF output signal drives the speaker. When the '1 + 2' LED is lit, the VF signal supplied by both DS0 channel decoders are combined.

2 **VOLUME** -- This control is used to adjust the loudspeaker volume. When the knob is rotated fully counterclockwise, the speaker is turned off.

DS1 TRANSMIT 1 SECTION

2.2.3

1 **Channel Number** -- This two-digit LED display shows the selected channel number. Any one of 24 channels may be chosen, and an extra channel position is also available (marked -- on the display). When this position is selected, the Channel Selection function is disabled.

2 **Channel Selection** -- Each depression of the UP or DOWN key changes the chosen channel by one number in the selected direction. Roll-over through an extra position (marked --) occurs between channels 1 and 24 when changes are made continuously in one direction. If the key is held down for over one second, the number selected change at the rate of 3 counts per second.

3 **MESSAGE INT** -- This LED is lit when the source of the message content of the selected DS0 channel is internal. This applies for both TONES and DATA. This LED is never lit when the MESSAGE EXT LED (4) is lit.

4 **MESSAGE EXT** -- This LED is lit when the source of the message content of the selected DS0 channel is external. This applies for both TONES and DATA. This LED is never lit when the MESSAGE INT LED (3) is lit.

5 **DATA** -- When this key is momentarily depressed, the DS0 channel content is selected from either the internal or the external DATA source as reflected by the lit

LED (3) or (4). The depression of this key also causes :

- the LED contained in this key to turn on with periodic short duration interruptions (*)
- the preemption of the screen in the Control & Measurements section to display either a message or a menu

6 **TONE** -- When this key is momentarily depressed, the DS0 channel content is selected from either the internal or the external TONE source as reflected by the lit LED (3) or (4). The depression of this key also causes :

- the LED contained in this key to turn on with periodic short duration interruptions (*)
- the preemption of the screen in the Control & Measurements section to display either a message or a menu

7 **EXT VF INPUT** -- When an external VF signal is plugged into this jack and the TONE key/LED is lit, the DS0 channel carries the digitally encoded VF signal applied to this input. At the same time the MESSAGE INT LED (3) is lit.

8 **EXT VF OVRL'D** -- This LED lights unconditionally when the VF signal level applied to the EXT VF INPUT jack (7) exceeds approximately 3.2 dBm. When this is the case, clipping of the applied signal results.

9 **SET/DIS'D** -- This key is only functional when the LED it contains is lit. When this is the case, the current DS0 channel selection is disabled. The momentary depression of this key causes the DS0 selection to be activated and the LED to turn off. The SET/DIS'D is used only while the Transmit 1 section operates in the THRU 1 mode. Refer to item 15 in this section for additional information.

10 **SIGNALING INT** -- This LED is lit when the source of the signaling content of the selected DS0 channel is internal. This applies for both STATE and telephone No. This LED is never lit when the SIGNALING EXT LED (11) is lit.

11 **SIGNALING EXT** -- This LED is lit when the source of the message content of the selected DS0 channel is external. This applies for both STATE and telephone No. This LED is never lit when the SIGNALING INT LED (10) is lit.

12 **No.** -- When this key is momentarily depressed, the VFDT is preempted to display the telephone number menu. From this menu a pre-stored telephone number can be selected or a new number can be composed. The selected number can then be carried by the selected DS0 channel either via the signaling bits (DP encoded No's) or the message bits (MF or DTMF encoded No's). The depression of this key also causes the built-in LED to take the FLOSO state (*)

13 **STATE** -- The momentary depression of this key is effective only if the Transmit 1 TONE key LED is lit. When this is the case, the momentary depression of the STATE key causes the state of the signaling bits A, B, C and D bits (A and B only when the current system selection is not ESF) in the DS0 channel to be selected from either the internal or the external signaling source as reflected by the lit LED (10) or (11). The depression of this key also causes :

- the LED contained in this key assumes the FLOSO state (*)
- the preemption of the screen in the Control & Measurements section to display the signaling bit status. The states may be changed by operating the soft key directly below the bit display on the screen.

14 **FORMAT** -- The momentary depression of this key causes the DS1 format selection to alternate between AMI and B8ZS as indicated by the associated lit LED. When the THRU mode prevails in the Transmit 1 section, this key is non-functional and the format selection

* The FLOSO acronym has been coined to simplify the reference to the state of the LED Flashing Long On Short Off.

* The FLOSO acronym has been coined to simplify the reference to the state of the LED Flashing Long On Short Off.

is controlled by the Receiver 1. In this case, the selected format is also displayed by the lit LED near the FORMAT key.

15 **THRU 1** -- Depression of this key selects the THRU 1 mode and causes the SET/DIS'D key/LED (9) to turn on. While the SET/DIS'D LED is lit, the content of every channel in the Transmit 1 PCM output bit stream is identical to the content of the channels in the DS1 bit stream monitored by the Receiver 1 section. The selection of the The THRU 1 mode also causes the VFDT to display the A & B signaling states in all 24 channels for the bit streams monitored by both DS1 Receivers.

While the THRU 1 mode prevails, an electronic interlock prevents the entry of any selection that could result in traffic disruption. Exit from the THRU 1 mode first requires the depression of the THRU 1 key and, within 700 milliseconds, the depression of the DS1 #1 key.

16 **DS1 #1** -- When this key is momentarily depressed, the VFDT is preempted to display the DS1 channelized bit stream menu. From this menu either the IDLE pattern or the 1005Hz @ -20 dBm0 tone can be chosen to fill all the other channels. The depression of this key also causes the built-in LED to take the FLOSO state (*)

17 **EXT DL SEL** -- This LED is lit when the external data link input access is selected. This LED can be lit only when the ESF or the SLC-96 system format is selected and pin 16 of J24 on the rear panel is grounded. When this pin is grounded and the ESF system format is selected and the YEL ALARM (18) code is being sent, this LED is off. This results because the data link is then preempted to carry the alarm code.

18 **YEL ALARM** -- Depression of this key toggles the function on and off. When on, the yellow alarm code is introduced into the outgoing bit stream. The yellow alarm code differs according to the system selection. When this selection is SLC-96, D1D, D2, or D3/D4, the code consists in forcing the state of the second most significant bit in every channel to zero. When the system selection is ESF, the code consists of a sequence of 8 consecutive 'one' bits followed by 8 consecutive 'zero' bits carried by the data link.

If the THRU 1 mode prevails, as indicated by the lit LED in the THRU 1 key, the depression of the YEL ALARM key does not cause the yellow alarm code to be sent. Instead, the LED in the THRU 1 key flashes twice to indicate the origin of the conflict. [Traffic disruption would result if the yellow alarm code were sent.]

19 **PCM OUTPUT MON** -- This jack accesses the T1 PCM output via two resistors of 430 ohms in the same manner as a monitor jack is placed across the line in the DSX-1 bay. When a 100 ohm termination is provided to this jack, the nominal level is -20 dB with respect to the normal level at the properly terminated T1 output jack.

20 **PCM OUTPUT T1** -- This jack delivers the bipolar formatted PCM bit stream generated by the Transmit 1 section. When terminated in 100 ohm resistor, the nominal level is 3.0 V base to peak.

DS1 TRANSMIT 2 SECTION

2.2.4

1 **THRU 2** -- Depression of this key selects the THRU 2 mode and causes the VFDT to display the DS0 selection screen. While the DISABLED heading in this screen is underlined, all 24 channels monitored by the DS1 Receiver 2 are passed through the DS1 Transmit 2 to the PCM output without interference. When the ENABLED heading is underlined, the content of 23 channels in the Transmit 2 PCM output bit stream are identical to the content of the same 23 channel numbers in the DS1 bit stream monitored by the Receiver 2 section. The channel No. selected by the receiver 2 carries the digitally encoded VF signal applied to the VF INPUT jack (6) in this section.

* The FLOSO acronym has been coined to simplify the reference to the state of the LED Flashing Long On Short Off.

While the THRU 2 mode prevails, an electronic interlock prevents the entry of any selection that could result in traffic disruption. Exit from the THRU 2 mode first requires the depression of the THRU 2 key and, within 700 milliseconds, the depression of the DS1 #2 key.

2 **DS1 #2** – When this key is momentarily depressed, the VFDT is preempted to display the menu of DS1 bit streams available for in-service or out-of-service testing. The depression of this key also causes the built-in LED to take the FLOSO state (*)

3 **LOOP DOWN** – When this key is momentarily depressed while the Transmit 2 is not in the THRU 2 mode, the built-in LED takes on the FLOSO state (*) and the VFDT is preempted to display the loop down code menu. From this menu either the prestored CSU, NI or user defined code can be selected or a new code can be composed. The selected code can be delivered to the T1 OUTPUT jack (7) for a set duration exclusively of any other bit pattern.

If the Transmit 2 is in the THRU 2 mode when the LOOP DOWN key is depressed, the LED in the THRU 2 key flashes twice to flag the origin of the conflict.

4 **LOOP UP** – When this key is momentarily depressed while the Transmit 2 is not in the THRU 2 mode, the built-in LED takes on the FLOSO state (*) and the VFDT is preempted to display the loop up code menu. From this menu either the prestored CSU, NI or user defined code can be selected or a new code can be composed. The selected code can be delivered to the T1 OUTPUT jack (7) for a set duration exclusively of any other bit pattern.

If the Transmit 2 is in the THRU 2 mode when the LOOP UP key is depressed, the LED in the THRU 2 key flashes twice to flag the origin of the conflict.

5 **ERROR** – When this key is momentarily depressed the built-in LED takes on the FLOSO state (*) and the VFDT is preempted to display the error menu. From this menu one can select both the type of errors to be injected in the bit stream delivered by the OUTPUT T1 jack (7) and the injection rate.

CONTROL & MEASUREMENT SECTION

2.2.5

1 **HELP** – This key, when depressed summons the VFDT to display a context-sensitive message designed to clarify and assist the user. When the design team could not think of a useful message, a number is displayed instead to allow a user to identify the screen when making either a suggestion or an inquiry to T-COM. Upon release of the HELP key, the previously displayed screen is displayed again.

2 **SYST** – A momentary depression of this key enables the user to either view the current system format and/or to change it. The system format selection includes SLC-96, D1D, D2, D3/D4 and ESF. The current selection is underlined; to change it, it is necessary to reset the instrument by simultaneously depressing both keys labeled RESET in the keypad. Additional information is provided in chapter 3.

3 **MODE** – A momentary depression of this key causes the VFDT to display the MODE menu. This menu lets you :

- enable or disable the beeper
- initialize the built-in clock and calendar
- set the DS0 channel protection

The menu provides easy-to-follow directions to use these features. Additional information is provided in chapter 3.

4 **TEST TIME** – A momentary depression of this key causes the VFDT to display the elapsed time since the beginning of a test sequence and to specify the duration of a test. When the preset time has been exceeded, the detected impairment events are no longer processed and the impairment event count screens are frozen until the instrument is reset. Additional information is provided in chapter 3.

---

* The FLOSO acronym has been coined to simplify the reference to the state of the LED Flashing Long On Short Off.

5 **REMOTE** -- This LED is lit only when the printer/terminal attached to the printer port sends commands to the 440B or while the 440B operates under remote control (this requires option 07).

6 **STATS RCVR C** -- When the 440B is equipped with option 53A (the DS1C Monitor/Demultiplexer), a momentary depression of this key caused the VFDT to display the screen last accessed in the sequence of screens of DS1C transmission statistics. If the 440B is not equipped with the 53A, this key is not functional.

7 **STATS RCVR 1** -- A momentary depression of this key causes the VFDT to display the screen last accessed from the DS1 Receiver 1 transmission statistics menu.

8 **STATS RCVR 2** -- A momentary depression of this key causes the VFDT to display the screen last accessed from the DS1 Receiver 2 transmission statistics menu.

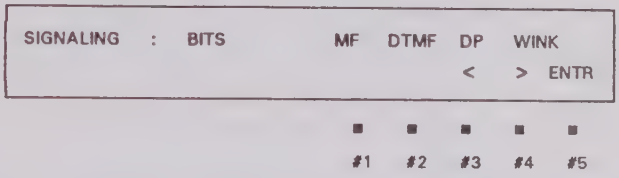
9 **DS0 DATA** -- A momentary depression of this key causes the VFDT to display the screen last accessed in the sequence of screens characterizing the DATA in the DS0 channel selected from the bit stream monitored by either DS1 Receiver 1 or 2.

10 **DS0 VF** -- A momentary depression of this key causes the VFDT to display the screen last accessed in the sequence of screens characterizing the VF signal in the DS0 channel selected from the bit stream monitored by either DS1 Receiver 1 or 2.

11 **DS0 SIG** -- A momentary depression of this key causes the VFDT to display the screen last accessed in the sequence of screens characterizing the signaling in the DS0 channel selected from the bit stream monitored by either DS1 Receiver 1 or 2.

12 **#1 - #5** -- The assignment of these so-called softkeys is defined from screen to screen by the labels located immediately above each key on the second line of the screen. For example in the screen [1] below, softkey #1 and #2 have no meaning and are thus not functional; softkey #3 acts as the left pointer, softkey #4 as the right pointing arrow and softkey #5 as the ENTER key.

Screen [1]



13 **ALT** -- When momentarily depressed, the LED in this green colored key is lit. When this LED is lit, the ALTernative (green) labels on the adjacent keypad (14) are active. The depression of any key on the key pad causes the LED to turn off. When this LED is turned off, the black labels on the keypad are active instead.

14 **Keypad** -- The dual color markings associated with each of the 12 keys of this keypad indicate the dual function. The green markings are active when the ALT key (13) is lit. When this key is not lit, the black markings are active instead. This keypad is used primarily for entering sequences of digits or other symbols used for sending telephone numbers or setting tone level and frequency etc. The * and the # keys play yet another role : when depressed simultaneously, the instrument is reset. The resetting causes all event counters to be cleared and the test timer to be reset to 00:00.

15 **Photo resistor** -- This device monitors the ambient lighting condition and controls the brightness of the VFDT. This ensures an optimal brightness under all practical conditions.

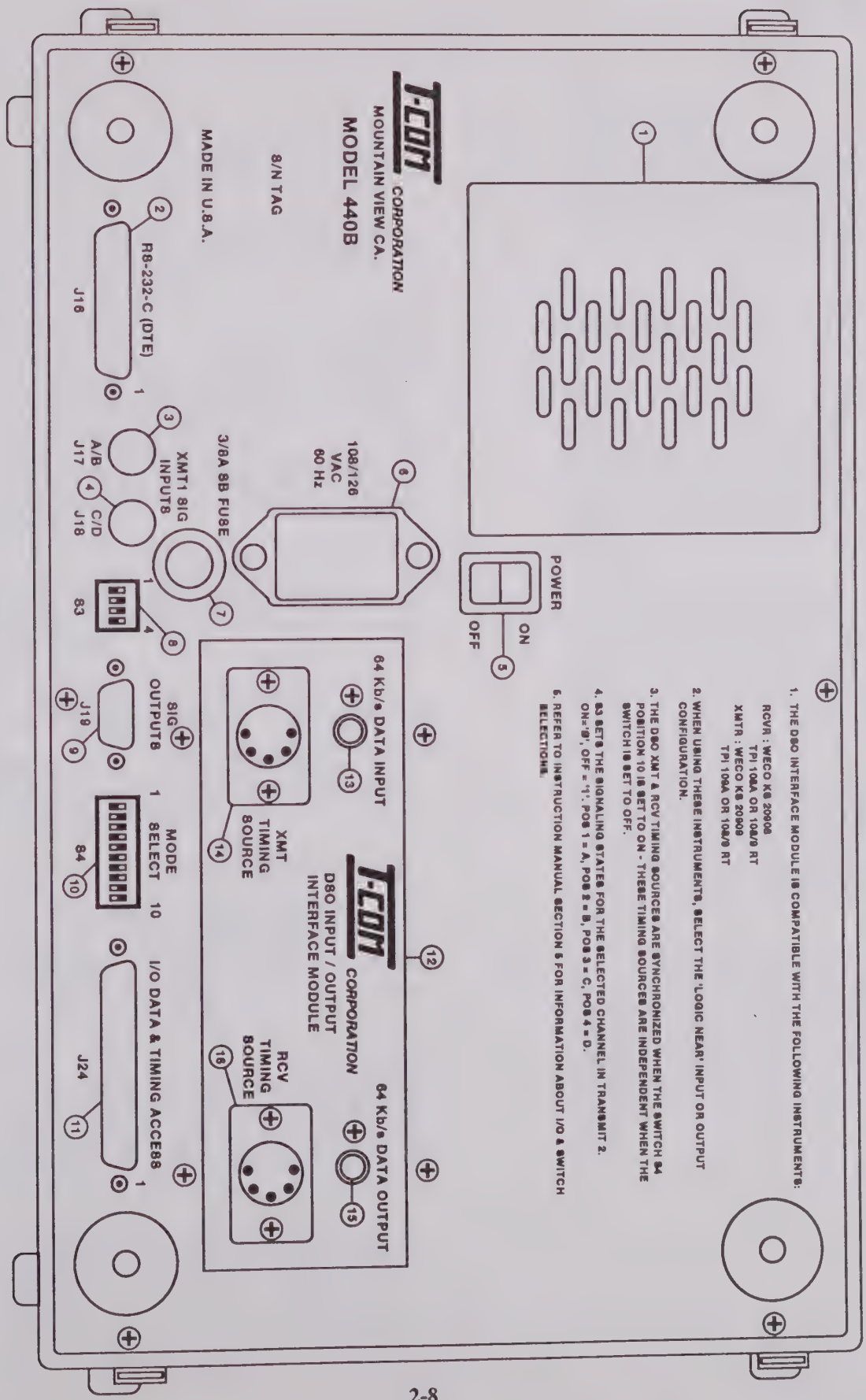

1. THE D80 INTERFACE MODULE IS COMPATIBLE WITH THE FOLLOWING INSTRUMENTS:
RCVR : WECO KS 20908
TPI 106A OR 102/9 RT
XMTR : WECO KS 20909
TPI 106A OR 102/9 RT
2. WHEN USING THESE INSTRUMENTS, SELECT THE 'LOGIC NEAR' INPUT OR OUTPUT CONFIGURATION.
3. THE D80 XMT & RCV TIMING SOURCES ARE SYNCHRONIZED WHEN THE SWITCH S4 POSITION 10 IS SET TO ON - THESE TIMING SOURCES ARE INDEPENDENT WHEN THE SWITCH IS SET TO OFF.
4. S3 SETS THE SIGNALING STATES FOR THE SELECTED CHANNEL IN TRANSMIT 2.
ON='0', OFF = '1'. POS 1 = A, POS 2 = B, POS 3 = C, POS 4 = D.
5. REFER TO INSTRUCTION MANUAL SECTION 5 FOR INFORMATION ABOUT I/O & SWITCH SELECTIONS.
T-COM CORPORATION
MOUNTAIN VIEW CA.
MODEL 440B
S/N TAG
MADE IN U.S.A.
3/8A 8B FUSE
108/126 VAC 60 Hz
POWER
ON
OFF
RS-232-C (DTE)
J16
XMT1 SIG INPUT8
A/B J17
C/D J18
S3
SIG OUTPUT8
J19
64 Kb/s DATA INPUT
XMT TIMING SOURCE
T-COM CORPORATION
D80 INPUT / OUTPUT INTERFACE MODULE
64 Kb/s DATA OUTPUT
RCV TIMING SOURCE
MODE SELECT
S4
I/O DATA & TIMING ACCESS
J24

Figure 2-2. Rear Panel

REAR PANEL FEATURES

2.3 In the description below, the numbers match the circled numbers in figure 2.2.

1 **Speaker assembly** -- This area must be kept clear of obstructions as the sound might otherwise be muffled.

2 **RS-232-C I/F** -- This 25 position female connector provides the interface required for the interface with a printer or a modem. Detailed information regarding this interface can be found in chapter 17.

3 **XMT 1 SIG A/B** -- This 310 type jack allows you to supply externally the A and B signaling states in the Transmit 1 selected DS0 channel.

4 **XMT 1 SIG C/D** -- This 310 type jack allows you to supply externally the C and D signaling states in the Transmit 1 selected DS0 channel.

5 **POWER ON/OFF** -- This is the power switch for the instrument.

6 **108/126 VAC** -- This three-prong inlet is used to connect the supplied AC power cord to a commercial AC source.

7 **Fuse** -- 3/8A Slow-blow is recommended.

8 **S3** -- This 4-position DIP switch is used for setting the A, B, C and D signaling states in the Transmit 2 selected channel. Additional information regarding the setting of this switch is found in chapter 12.

9 **J19** -- This 9-position female connector provides access in real-time to the signaling states associated with the selected DS0 channel in each DS1 Receiver. Additional information on this connector is found in chapter 19.

10 **S4** -- This 10-position DIP switch is used for selecting the printer port baud rate, to select the PCM output format on Transmit 2, to select the duration of the LED test, to calibrate the real-time clock and to select the DS0 interface timing mode. Additional information regarding this switch is found in chapters 3 and 17.

11 **J24** -- This 37-position female connector provides access in real-time to timing signals associated with the two DS1 Receivers and with Transmit 1. Additional information on this connector is found in chapter 19.

12 **DS0 Optional panel** -- When the DS0 interface, option 03, is not installed, this cavity is covered with a blank panel.

13 **64 kb/s DATA INPUT** -- When an external 64 kb/s data stream is plugged into this jack and the Transmit 1 DATA key/LED (5) is lit, the DS0 channel carries the stream applied to this input. At the same time the MESSAGE INT LED (3) is lit. Additional information on this connector is provided in chapter 10.

14 **XMT TIMING SOURCE** -- This source delivers the 8 and 64 kb/s clock signals required to synchronize the externally supplied 64 kb/s stream to the bit stream delivered by the Transmit 1 section. Additional information on this connector is provided in chapter 10.

15 **64 kb/s DATA OUTPUT** -- This delivers a unipolar formatted copy of the 64 kb/s stream obtained in the selected DS0 channel from either DS1 RCVR 1 or 2. Additional information on this connector is provided in chapter 5.

16 **RCV TIMING SOURCE** -- This source delivers the 8 and 64 kb/s clock signals required by a data test set to properly identify each bit in the bit stream delivered by the 64 kb/s DATA OUTPUT jack (15). Additional information on this connector is provided in chapter 5.

3. GETTING STARTED

INTRODUCTION

3.1 This chapter contains important information about the setting-up and the preparation for use of the 440B. Additionally, this chapter describes the self-diagnostics procedure executed automatically at power-up as well as the operation of the four system-level keys in the Control & Measurements section.

SETTING-UP AND INITIALIZING THE 440B

3.2 **- Physical considerations**

Because the 440B does not contain any position sensitive components, it may be operated in any position. Typically, it is used either placed vertically on the floor of the office, resting on its rear panel legs, or lying horizontally on a cart or shelf. Alternatively, the 440B can be rack mounted. To this end, a set of rack mounting brackets can be secured to each side of the instrument. Refer to chapter 20 for installation instructions.

When operating the 440B, one must be sure not to obstruct air flow through its side vents as this may cause undesirable heat build-up. In particular, the 440B should not be operated while in its canvas carrying case.

CAUTION

If the set is exposed to excessive humidity the application of power can be dangerous both to the instrument and to the personnel using the set.

- Powering considerations

To power the set, one end of the AC power cord supplied with the instrument must be plugged to the rear panel AC inlet and the other end to a power line outlet. To operate properly, the AC line voltage at the power cable outlet must be in the range of 108 to 126 VAC. As a general rule, it is not advisable to use long extension cords as these may cause significant voltage drops and result in unsatisfactory operation of the set. The set is powered-up by setting the rear panel power switch to ON.

- Selecting operating modes

The 440B operating mode should be selected prior to powering-up the set. The operating mode selection is performed by setting the 10 position DIP switch (S4) on the rear panel appropriately.

The switch positions requiring setting prior to power-up are: 5, 6 and 8. All the other selections can be made as required; their description is given in the chapters listed in table 3.1.

S4/5 controls the duration of the LED test carried-out as part of the execution of the self-diagnostics routine. When S4/5 is set ON, these LED's remain turned on for about 10 seconds prior to turning off. When this switch is set to OFF, the duration is only 3 seconds.

S4/6 enables the downloading to battery protected RAM of the factory selections for the test tone sequence, the telephone number sequence, the loop codes, the data test byte and the 24 bit test sequence. When prior to power-up S4/6 is set to ON, upon completion of the execution of the self-diagnostic routine, the EPROM stored factory selections are transferred to RAM, replacing the current RAM content. Upon completion of the transfer, the user is prompted by a screen to place S4/6 back to the OFF setting. [If S4/6 is in the OFF setting upon power-up, the values in RAM are unaffected.]

S4/7 selects the VFDT symbols representing the ABCD signaling states. The 1/0 represents the logic states and the ■/. represents the corresponding lit/unlit LED states. In practice, the selection is a matter of personal preference.

S4/8 selects the real-time clock calibration mode. Unless calibration is to be performed, this switch must remain in the OFF setting.

Table 3.1 below identifies the function of each switch position.

Position	ON	OFF	Comments	Chapter
1	-	-	N/A	-
2	Baud rate sel		RS-232-C	17
3	Baud rate sel		RS-232-C	17
4	Baud rate sel		RS-232-C	17
5	Slow	Fast	Self-test	-
6	Factory setting		Norm.	-
7	1/0	■/.	-	7
8	RTC CAL		Normal	23
9	-	-	N/A	-
10	SYNC	ASYNC	DS0 CK	10

Table 3.1 S4 Selection Listing

- SELF-DIAGNOSTICS CAPABILITY DESCRIPTION

3.3 Upon power-up the 440B automatically executes a comprehensive self-diagnostic routine. This routine verifies the operational integrity of every microcontroller in each system subassembly. If a non-catastrophic operational difficulty is encountered, the execution of the self-diagnostic routine is suspended and a message indicating the nature of the problem is displayed by the vacuum fluorescent display tube (VFDT). At this point the user has the choice to use the set in spite of the identified problem or to take corrective action. As an example, the screen [1] below shows the message displayed when the routine detects an operational failure of the frame loss latch in Receiver 2.

Screen [1]

```
RCX #2 FR LOSS latch failure.
To continue, press any key
```

Upon depressing a key, the main controller restores the execution of the self-diagnostic routine. The process just described is repeated if additional failures are detected.

If in the course of executing the self-diagnostics routine no failures are detected, all front panel LED's are turned on for the period of time selected by S4/5 and the VFDT displays a brief sequence of test screens. The screen [2] is then displayed for 3 seconds.

Screen [2]

```
The self-test routine is over.
All systems are GO !
```

If a failure was detected by the processor, the screen [3] is displayed for 3 seconds instead of screen [2].

Screen [3]

```
The self-test routine is over.
Corrective action should be taken.
```

When the 3 second time-out period is over, the VFDT automatically displays the second screen in the STAT/RCVR #1 menu and the instrument is reset. This reset causes all impairment counters to be cleared and the test timer to be set to 00:00. An example of the screen displayed at this point is shown by screen [4] below.

Screen [4]

```
D1 level          Frequency (Hz)
-0.3 dBDSX        1,544,012          NXT
```

- SYSTEM-LEVEL KEY OPERATION

3.4 The four keys located in the left side of the Control & Measurements

opposed to a local function. The operation of each of these keys is described below.

- HELP

While this key is held depressed, the VFDT is preempted to display a message intended to help the user in resolving operational difficulties with the instrument. The messages displayed typically indicate why a command cannot be executed, what option is required to carry-out specific tests or the acceptable range of parameters to be entered by the user. In some cases, when we could not think of a useful message, an ID number is displayed instead. Feel free to refer to this number in communicating to our service department personnel and to offer suggestions for appropriate and useful messages. Upon release of the key, the VFDT displays again the screen prevailing before the depression of the HELP key. An example of a HELP screen is shown in screen [1] below.

Screen [1]

```
To exit from THRU mode hit the THRU 1
key and then QUICKLY the DS1 #1 key
```

[This message is given following the unsuccessful attempt to exit from the THRU mode.]

- SYST

The current system format selection controlling both DS1 Receivers and both DS1 Transmitters can be viewed and changed, when desired. The SYST key, when momentarily depressed, causes the VFDT to display the current selection. An example of the screen displayed upon depressing the SYST key is shown in screen [2] below.

Screen [2]

```
D3/D4  To select another format,
       depress the two reset keys.                EXIT
                                                   ■
```

If the EXIT softkey in screen [2] is depressed, no change to the system selection is made and the screen prevailing before the SYST key was depressed, is displayed again.

If RESET is entered while screen [2] is displayed, screen [2] is replaced by the screen [3] illustrated on the following page.

Screen [3]

```
SYST :    SLC-96    D1D  D2  D3/D4ESF
                                        <   >  EXIT
                                        ■   ■   ■
```

[The current selection is underlined in the actual display.] The depression of the < or the > softkeys causes the underline to move to the next adjacent selection. At the same time, the actual system selection is changed to the underlined value. The SYST select mode is exited by depressing the EXIT soft key. If no entry of the < or the > softkeys was made, it is still necessary to depress the EXIT key to exit.

Upon exiting from the SYST menu, the RESET command is executed, the screen prevailing prior to the entry in the SYST menu is displayed again.

- MODE

The MODE key provides access to a menu of three useful functions

- ▸ setting of the built-in clock and calendar
- ▸ setting the DSO data measurement protection mode and
- ▸ controlling the beeper.

When the MODE key is momentarily depressed, screen [4] is displayed.

Screen [4]

```
Time/Date                    DS0 Protect(ON)
Beeper(OFF)                  ON   OFF   <   >   SET
                             ■    ■     ■   ■    ■
```

In the above screen [4], one of the headings is underlined (not shown). The ON, OFF and SET softkey headings are displayed only when appropriate. The < and > softkeys are used for indexing the underline.

The DS0 protection may be set (ON) or (OFF) by using the corresponding softkeys. The ON setting should be used when a DS0 data error measurement is to be performed and presumably not disrupted by inadvertent changes in switch settings. When the DS0 protection is set (ON), the following front panel controls are disabled :

- ▸ DS0 channel number selection in both Receivers and Transmitters
- ▸ Receiver selection when displaying DSO DATA, VF or SIG menus

▸ DS1 Transmit 1 DS0 channel content selection

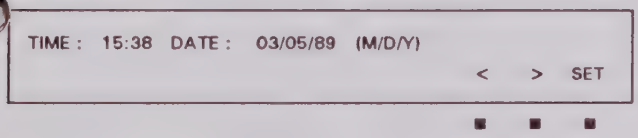
When the DS0 Protect selection is OFF, the restrictions above listed are lifted.

When the built-in beeper is enabled, each key depression is accompanied by one beep if the key entry is accepted or by two beeps if the key entry is rejected. This function can be disabled or enabled by underlining the Beeper heading with the help of the pointer softkeys and selecting either the OFF or the ON parameter respectively.

The built-in clock and calendar can be accessed and, when necessary, reset. This may be necessary when daylight saving time goes into effect, the instrument is transported across a time zone, or when the built-in rechargeable battery is disconnected.

To access the clock and calendar, the Time/Date heading must be underlined and the SET softkey momentarily depressed. This causes the display of screen [5] with of course different values for the time and the date.

Screen [5]



The desired time and date are obtained by using the keypad on the right side of the VFDT to enter each digit at the location pointed by the underline. When the entry is completed, the SET softkey is momentarily depressed to activate the selection and exit the screen. If an out-of-range value is entered, the depression of the SET key does not cause this value to supersede the pre-existing one and the screen [6] is displayed for 3 seconds.

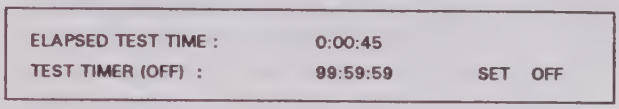
Screen [6]

- TEST TIME

This key accesses two features : the display of the time elapsed since the most recent reset of the instrument and the setting of a test time period.

When the TEST TIME key is momentarily depressed, the VFDT displays a screen similar to screen [7] below.

Screen [7]



The two softkeys SET and OFF provide for setting the test timer to the desired time (00:00:00 to 99:59:59) or disabling the timer. Upon depressing the SET key, a screen similar to screen [8] replaces screen [7].

Screen [8]

The desired time is obtained by using the keypad on the right side of the VFDT to enter each digit at the location pointed by the underline. When the entry is completed, the test timer is started by entering the RESET. It should be noted that screen [8] displays the test time, not the remaining time in the test; therefore this time is not decremented after the start of the test. When during a test, the timer times out, all the impairment event counters stop tallying new counts and all error rate values at that time are frozen.

The timer may be turned off at any time while screen [7] is displayed by depressing momentarily the OFF softkey. Screens [7] and [8] are exited by simply requesting any other screen.

- FLOSO

The 440B front panel has 15 menus each controlled by a dedicated key. To indicate the menu from which the current screen is obtained, the LED in the selected menu key is steadily lit except for brief interruptions at regular time interval. This state is referred to as FLOSO for Flash Long On Short Off. As different menu keys are depressed, the FLOSO state jumps along from selection to selection thus providing a helpful reminder.

4. DS1 MONITORING AND PERFORMANCE ANALYSIS

INTRODUCTION

4.1 The 440B is equipped with two DS1 Receivers to provide, among other things, the real-time monitoring and the transmission performance evaluation of two DS1 formatted signals at the same time. In this chapter you will find :

- an overview of real-time DS1 transmission monitoring
- directions to set-up the 440B for DS1 monitoring
- a description of the real-time DS1 diagnostic capability
- a description of the DS1 impairment data measurements
- in-service monitoring application information

REAL-TIME DS1 TRANSMISSION MONITORING

4.2 DS1 monitoring is performed independently by each of the two DS1 Receivers. Each of these Receivers can accept a DS1 formatted bit stream as found typically at the DSX-1 bays and display in real-time the occurrence of a number of transmission impairments. The two Receivers operate independently of one another but provide for the direct comparison of clock rate between monitored bit streams to display in real-time the bit-by-bit slippage. Additionally, the two receivers allow for the real-time comparison of transmission impairments on two lines whether from the same system or from different ones.

SETTING-UP THE PCM INPUT SELECTION

4.3 Each DS1 Receiver PCM input jack can be configured to accept the signal found at a monitor jack, at a bridging jack or at an input/output jack. The 440B PCM inputs are independently configured by setting the INPUT SEL switch next to the input jacks as follows :

Jack type	Selection	Impedance (Ohms)
input	TERM	100
output	TERM	100
bridging	BRDG	1000
monitor	MON	100

Remarks

- The 440B tolerates up to 800 pF cabling capacitance at the input jack. Considering that a typical patch cord has 20 to 25 pF per ft, the patch cord length should not exceed about 30 feet.

- The PCM INPUT SEL switch is active only when a plug is inserted in the corresponding input jack. When for example the input signal is obtained internally from the options 52B or 53A, this selection is ineffective.

Although primarily intended to be connected to dry circuits, the 440B PCM input jacks can be patched to simplex powered lines if simple precautions are taken.

CAUTION

The 440B signal access jacks are designed to be patched to circuits protected from lightning surges and exhibiting voltages not exceeding 250 volts with respect to earth ground. The application of voltages in excess of 250V can be dangerous both to the instrument and to the personnel.

Before patching either 440B input jack to wet circuits, it is highly recommended to ensure that the instrument is properly grounded to the AC power line via the power cord. If the power cord is frayed or is in poor condition, it should be replaced. Furthermore, to prevent shorting the line to ground, the order of patching an input to the line should be: patching to the 440B first, patching to the live circuit last.

PERFORMING REAL-TIME PCM TRANSMISSION MONITORING

4.4 When the 440B PCM input selection is properly set, the DS1 Receiver analyzes the applied PCM signal and displays in real-time the status with both dedicated LED's and the VFDT.

LED DISPLAY

4.4.1 The diagnostic information supplied by each LED is given below.

NO PCM LED :
- ▸ is off when the minimum 'ones' density requirement is met
- ▸ flashes on when a string in excess of 15 consecutive 'zeros' is detected
- ▸ is on continuously when no signal is applied or if the signal amplitude is below the minimum acceptable or if the line is said to be oscillating

BPV LED :
- ▸ is off when no bipolar violations are detected
- ▸ flashes on briefly for each detected bipolar violation
- ▸ is steadily on for signal of excessive amplitude (input circuit overload) or when the BPV density exceeds 20/second

CRC ERR LED :
- ▸ is off when the system selection is not ESF or when the system selection is ESF and no CRC code error is detected or framing is lost
- ▸ flashes on briefly for each detected occurrence of a CRC code error
- ▸ is steadily lit when the CRC code error rate exceeds 20 per second

FR BIT ERR LED :
- ▸ is off when the frame loss condition prevails or in the absence of frame bit errors when framing prevails
- ▸ flashes on briefly for each detected occurrence of a frame bit error
- ▸ is steadily lit when the frame bit error rate exceeds 20 errors per second

FR LOSS LED :
- ▸ is off when framing prevails
- ▸ flashes on briefly each time framing is lost and quickly reacquired
- ▸ is on while framing is lost

ALL ONES :
- ▸ is off when framing prevails or while the all-ones code is not detected
- ▸ is on only after this code has been detected for over 40 ms nominal

YEL ALM :
- ▸ is on only when the SF yellow alarm code is present for over 30 ms or when the ESF yellow alarm code is repeated at least 14 consecutive times
- ▸ is off otherwise

SYNCH/BIT ERROR LED :
- ▸ is lit green when a synchronization on a known pattern prevails
- ▸ flashes red for each detected bit error once pattern synchronization prevails
- ▸ is steadily lit red when the bit error rate exceeds 20 errors per second while pattern synchronization prevails
- ▸ is turned off otherwise

B8ZS LED :
- ▸ is lit when the monitored bit stream contains the B8ZS code at least once per 100 ms.

VFDT DISPLAY

4.4.2 Additional DS1 measurements displayed in real-time by the VFDT are given below. These measurements are obtained by momentarily depressing the key labeled STATS/RCVR 1 or the key labeled STATS/RCVR 2 located below the VFDT.

- ▸ **DS1 Level measurement**
  The amplitude of the PCM signal presented to each DS1 Receiver input is measured on an on-going basis. The display of the obtained base-to-peak value is updated once per second. The measurement is expressed in dBDSX regardless of the INPUT SEL switch setting. When the level is measured while the input selection is MON, 20 dB are added to the level reading. A reading of 0.0 dBDSX corresponds to a nominal base to peak pulse amplitude of 3.0V. An example of the DS1 Level/Frequency screen [1], obtained when PCM is applied, is shown below.

Screen [1]

DS1 level	frequency (Hz)	
-0.2 dBDSX	1,544,014	NXT

- ▸ **DS1 Frequency measurement**
  The frequency of the PCM signal presented to each DS1 Receiver input is measured on an on-going basis. The display of the obtained value is updated once per second. The measurement is expressed in Hz. The acceptable frequency range is nominally 1.544 MHz ± 10 KHz. To hold its accuracy, the measurement requires that the input voltage base-to-peak value be in the range 2 to 4 volts for

TERM and BRDG and 200 to 400 mV for the MON setting.

▸ **DS1 Slippage display**
The bit-by-bit display of the slippage is obtained in real-time when both Receivers are monitoring a PCM bit stream and the NXT softkey in screen [1] above is momentarily depressed. An example of the screen [2] display is given on the following page.

Screen [2]

The slippage display consists of a stack on the left and a scale under the SLIPPAGE heading. Together, the marker on the scale and the height of the stack represent the instantaneous delay between the bit positions selected on each of the two monitored PCM bit streams. When the two observed bit streams have precisely the same frequency and the instrument has been reset, the stack is empty and the marker sits on the middle of the scale.

If the frequency of the bit stream presented at the input of Receiver 1 is greater than the frequency of the bit stream presented at the input of Receiver 2, the stack increases in height one layer at a time, representing each time one bit of slippage. When the stack reaches its full height, it is emptied and the marker on the scale advances by one position. This process repeats itself until finally the marker falls-off the edge of the scale on the right and reappears again in the middle of the scale. At the same time, the SLIP COUNT is incremented. If the frequency of the bit stream measured by Receiver 1 is less than the frequency measured by Receiver 2, the process is reversed.

DS1 TRANSMISSION PERFORMANCE CHARACTERIZATION

4.5 The impairment activity displayed by the LED's in each Receiver section is also captured by a dedicated processor to compute a number of transmission performance indices. The following sections cover the definition of these measurements and how to access them.

DS1 PERFORMANCE INDEX DEFINITIONS

4.5.1 The 440B impairment data processor computes the indices listed in table 4.1. This table provides the definition and the range of values for each index. Additional background information regarding some of these measurements are also included.

Index	Definition	Range
BPV	count	0 to 9999
FR BIT ERR	Frame bit error count	0 to 9999
CRC ERR	CRC-6 error count	0 to 9999
FR L-SEC	seconds w/ lost framing	0 to 9999
ERR-SEC	seconds w/one or more BPV's PCM loss or CRC error occurrences exclusive of SES	0 to 9999
SES	seconds in which one or more of the following occurred - over 320 CRC errors - over 1544 BPV's - over 12 frame bit errors - frame loss	0 to 9999
CSES	3 or more consecutive SES's	0 to 9999
YEL-ALM-SEC	seconds in which the yellow alarm occurred	0 to 9999
AIS-SEC	seconds in which the all ones code occurred	0 to 9999
FBER	Frame bit error rate # FR Bit ERR's /# FR's	1.0×10^{-3} to 0.1×10^{-9}
CBER	CRC-6 bit error rate # CRC ERR's/# bits	1.0×10^{-3} to 0.1×10^{-9}
BER	Bit error rate #Bit ERR's/# bits	1.0×10^{-3} to 0.1×10^{-9}
SLIP COUNT	absolute # of slipped bits/193	0 to 9999

Table 4.1 Index definitions and ranges

▸ **CRC Errors**

This type of errors can only be found when monitoring ESF formatted bit streams. An error is detected when the 6-bit signature received along with an extended superframe does not match the 6-bit word computed by the Receiver for the same extended superframe. When this is the case, it is accurate to state that one or more bits have been corrupted in a block of 4614 bits.

> **Note:** CRC errors are only counted when there is framing. If framing is lost over a significant part of the monitored period, the CRC count is then lower than fact.

▸ **Frame Bit Errors**

For any system selection, framing bit errors FT are monitored and captured. Framing bit error counting is disabled during framing loss to avoid false counting. If framing is lost over a significant portion of the monitored period, the frame bit error count may be lower than fact.

▸ **Frame loss-seconds**

The frame loss-second counter increments by one count for each second during which framing is lost when a plug is inserted in the PCM input jack. The frame loss count is incremented whether the frame loss exists for only a small fraction of a second or for a very long time. Under ordinary conditions, frame loss occurs primarily as a result of substantial burst-error activity, or when the PCM signal is lost.

> **Note:** A frame loss is defined as 2 frame bits in error in a group of 5 frame bits.

DS1 TRANSMISSION PERFORMANCE MEASUREMENT DISPLAY

4.5.2 By momentarily depressing the STATS/ RCVR 1 or 2, you can display all the DS1 measurements performed on the data collected by Receivers 1 or 2 respectively. The measurements are gathered as a series of screens. The successive screens are displayed by momentarily depressing the NXT softkey. An example of a screen sequence is shown by screens [3] through [7] on the following page.

Screen [3]

BPV	FR BIT ERR	CRC ERR	
3241	67	142	NXT

Because the CRC measurement is only meaningful when the instrument operates in the ESF format, this heading and the corresponding count are displayed only when the ESF system selection prevails.

Screen [4]

ERR-SEC	SEV E-S	CSV E-S	FR LOSS-SEC	
377	116	5	12	NXT

The depression of the NXT softkey in screen [4] yields a screen similar to screen [5].

Screen [5]

YEL ALM-SEC	AIS-SEC	
33	0	NXT

The depression of the NXT softkey in screen [5] yields a screen similar to screen [6].

Screen [6]

FBER	CBER	
2.3-8	2.9-8	NXT

If the format selection is not ESF, the CBER header and its corresponding data field are blanked out.

When in the STATS/RCVR 2 menu only, if option 05 is installed and the current DS1 #2 bit stream selection is any repeating test pattern (3/24, QRS, all ones, 1/8 or user-defined 24-bit sequence), upon depressing the NXT softkey in screen [6], the VFDT displays a screen similar to screen [7] below.

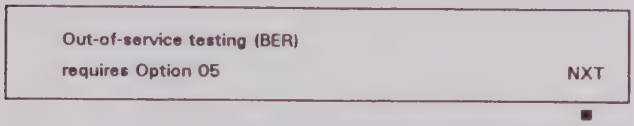
Screen [7]

BIT ERR	SYNC L-SEC	BER		
314	12	3.1-8	PAT	NXT

If the pattern monitored by Receiver 2 is not a repeating sequence, the values shown in screen [7]

are replaced by 'N/A' standing for 'not applicable'. If alternatively, option 05 is not installed, screen [8] is displayed when the NXT softkey is momentarily depressed in screen [6].

Screen [8]



When depressing the PAT softkeys in screen [7], the current DS1 #2 selection in the DS1 Transmit 2 section is displayed. Additional information regarding out-of-service testing is found in chapter 16.

IN-SERVICE MONITORING APPLICATION INFORMATION

4.6 In recent years, in-service testing has become increasingly popular. This has come partly from the recognition of the measurement validity and usefulness and from the frequent impracticality of turning a system down to perform traditional out-of-service testing. This section discusses a number of in-service testing related issues as well as the applicability of the measurements described in the previous sections.

IN-SERVICE BER MEASUREMENT

4.6.1 Although BER measurement is generally thought of as an out-of-service based measurement, it is possible to obtain an excellent estimation of the true bit error rate sustained by the DS1 formatted transmission without interfering with the traffic. Three methods yielding indirect BER measurements are discussed in this section.

▸ **BPV Event Counting**

Because higher level multiplexers (M12, M13 and above) are not transparent to BPV's, the BPV's observed on a circuit must have been created in the transmission segment from the test point to the nearest multiplexer. As a consequence, the counting of BPV's offers a handy way of delimiting the location of an impairment source to a specific link in the network.

An excellent correlation exists between BPV rate and bit error rate (BER) when the BPV rate is 10^-3 or less. When the error rate is greater than 10^-2, cancellation of BPV's occur more frequently. This yields a less accurate (or more favorable) BER measurement.

▸ **CRC based BER (CBER)**

When monitoring ESF formatted DS1 transmission, the CRC-6 error rate yields a good approximation of the actual bit error rate when the observed rate is 10^-6 or smaller. When the BER is significantly greater than this value, the accuracy is reduced. This results from the fact that a CRC error is declared when one OR MORE bit errors have been introduced in a field of 4632 bits (24 frame/ESF). When the error rate decreases, so does the probability that more than one bit error occurs in a block of 4632 bits, and thus 1 CRC error is more likely to represent 1 bit error. In short, the CBER is a dependable BER measurement when the CBER is 10^{-6} or smaller. The main shortfall of this measurement is that it only applies to ESF formatted DS1 transmission.

▸ **Frame bit based BER (FBER)**

The computation of the FBER by the 440B yields a very good estimate of the true BER and is applicable to both SF and ESF formatted DS1 bit streams. The main disadvantage of this technique is that it requires typically a long test time when the BER is small (10^-8 or less). The usability of the FBER to characterize the entire bit stream rests on the observation that PCM transmission corrupts every bit with the same probability. As a consequence, the bit error rate computed for one bit is statistically the same as for all the other bits if the test period is sufficient. The required test period depends on the desired accuracy of the measurement and of the BER itself since a minimum number of errors must be observed to obtain a meaningful measurement. To help in determining the minimum required period of monitoring, refer to the graph in figure 4.1. The graph is based on the minimum time required to acquire 4 frame bit errors as a function of the anticipated BER for both SF and ESF formatted transmission. It should be noted that the values obtained from this chart are only minimum, and that overall measurement accuracy is always increased by exceeding the given values.

To use the graph in figure 4.1, select the expected BER on the vertical axis and extend a horizontal line to the slanted line corresponding to the transmission format used. Mark the intersection with a dot. A line drawn vertically from the dot to the horizontal axis yields the minimum needed test time.

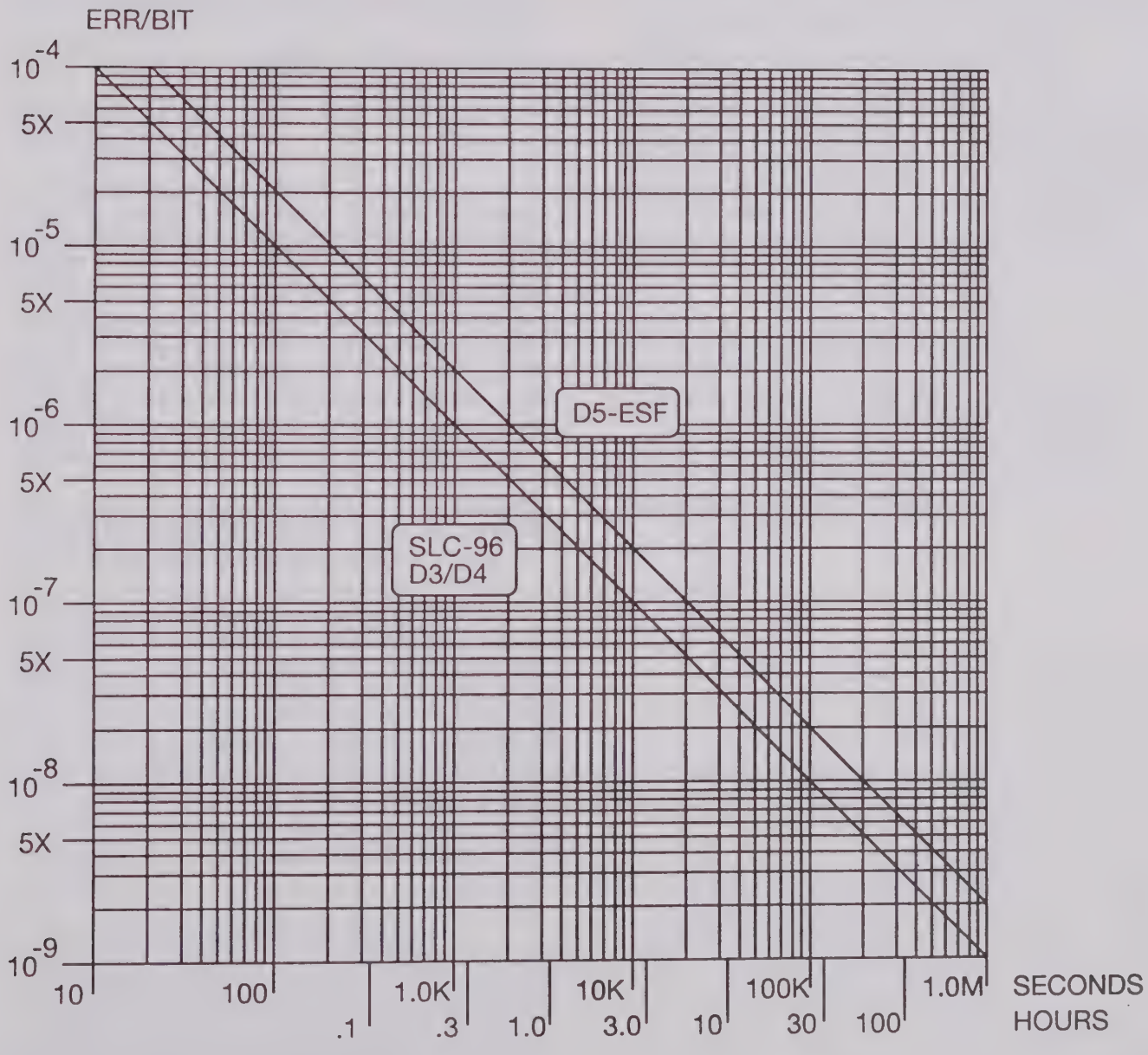


Figure 4-1. Minimum Required Test Time

For example, if a D3/D4 system is expected to exhibit an average bit error rate of 5 x 10-7 errors/bit, the minimum required observation time is approximately 2000 seconds (just over 1/2 hour).

SLIPPAGE MEASUREMENT APPLICATIONS

4.6.2 The bit slippage display capability built-in the 440B has a number of practical applications. Some of the most useful ones are described in this section.

▸ **Loop timing integrity check**
The loop timing integrity of a channel bank can be performed without taking the bank out of service by simply monitoring the XMT and RCV bit streams simultaneously with the two Receivers. Timing integrity is indicated when no shift in the slip display marker is observed over an extended period of time. To simplify the observation, it is best to reset the 440B after the two PCM signals are applied to the PCM inputs and to note that the stack remains empty and the marker stays on the mid point of the scale.

Lack of loop timing or loss of phase locking integrity is normally evidenced by a drift of the marker in one direction at a relatively constant rate.

▸ **Stuffing/destuffing process integrity check**
The integrity of the stuffing and destuffing process performed by high level multiplexer when combining asynchronous DS1 bit streams can be verified by comparing the average clock rate of the DS1 bit stream before multiplexing with the average clock rate of the DS1 digroup in the multiplexed bit stream. The use of 53A (for M1C multiplexers) or 52B (M13 multiplexers) is required. The test is identical to the loop timing integrity check discussed in the previous paragraph.

▸ **Jitter and frequency wander detection**
When jitter or frequency wander takes place between two PCM bit stream clock frequencies, the slippage marker position and the level of the stack are forever randomly changing. The position of the marker or the size of the stack only provide qualitative information of the amount of jitter. However, the magnitude of the frequency wander (in bits) can be readily evaluated by noting the peak-to-peak magnitude of the displacement of the marker on the scale.

▸ **Frame slip counting**
The frame slip counting capability offered by the 440B is based on the premise that one frame slip count accrues when 193 bits of slippage have accumulated between the two monitored bit streams. In the absence of known standard, this number of bits has been arbitrarily selected. In practice, different digital switch makers have arbitrarily selected different values to reflect the underflow or the overflow of a buffer whose length may be 256 bits, 512 bits or yet other values. Consequently, 'frame' slip counts on the 440B may differ significantly from the counts observed by the digital switch without raising a suspicion that either machine is defective. On the other hand, if one machine indicates a significant number of slips, say 10 or 12, and the other indicates 0, one of the two machines is suspect.

IMPAIRMENT DATA RECORDING

4.6.3 When the 440B is equipped with option 04, a time and date stamped record of the impairment activity monitored by the 440B can be obtained. Additional information on the use of this capability is provided in chapter 17.

5. DS0 CHANNEL DATA MEASUREMENTS

INTRODUCTION

5.1 The content of the 64 kb/s DS0 channels selected from either DS1 Receiver 1 or 2 can be displayed in real-time by the VFDT and when the 440B is equipped with option 05, a number of transmission performance measurements can be performed on this data without requiring additional equipment. When it is necessary to analyze the data content at the DS0 subrate level or to perform protocol level testing, an optional DS0 data interface unit can be added to the 440B to attach these specialized instruments. In this chapter, you will find:

- an overview of DS0 data monitoring and measurement capability
- directions to set-up the 440B for DS0 data monitoring
- a description of the real-time DS0 monitoring capability
- a description of the DS0 transmission performance evaluation
- a description of the optional (RCV) DS0 data interface
- DS0 data measurement application information

DS0 DATA MONITORING/MEASUREMENT CAPABILITY OVERVIEW

5.2 The DS0 Data Monitoring and Measurement capabilities offered by the 440B include:

- the display of a continually updated histogram representing the average state of each of the 8 bits in the 8000 bytes carried each second by the DS0 channel
- the detection and the counting of bit errors for selected bit patterns (requires option 03)
- the processing of the error counts to yield DS0 transmission performance indices

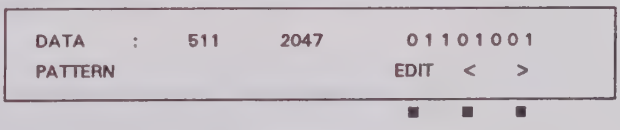
All these measurements are readily obtained via the VFDT once the 440B is appropriately set-up.

SETTING-UP THE DS0 CHANNEL MONITORING MODE

5.3 To monitor the content of a DS0 channel, it is necessary for the DS1 Receiver to receive a DS1 formatted bit stream and to let the 440B system format match the format of the monitored DS1 bit stream. In addition, the DS1 Receiver PCM input selection must be set according to the PCM signal source as described in chapter 4. The desired channel is selected on the DS1 Receiver by using either switch located under the channel No. display.

To detect bit errors, the built-in DS0 pattern analyzer must be instructed to recognize a specific 64 kb/s test pattern. This is accomplished by selecting the DS0 internal DATA menu in the Transmit 1 section. When a plug is not inserted in the 64 kb/s DATA INPUT jack on the 440B rear panel (P/O option 03), the momentary depression of the DATA menu/key in the Transmit 1 section causes the VFDT to display a screen similar to screen [1].

Screen [1]



The current selection is underlined. By momentarily depressing either pointer softkeys, the underline can be moved right or left to select either the pattern 511, the pattern 2047 or the user-defined byte.

The 511 pattern, sometimes referred to 2^9-1, is a pseudo-random 64 kb/s pattern commonly used for DDS transmission testing. The 2047 pattern (2^{11}-1) is used for the same purpose but has a richer range of bit combinations. The 8-bit byte (01101001), when underlined, is repeated 8000 times per second to yield 64,000 bits. This byte can be changed to any combination of 1's and 0's as required by momentarily depressing the EDIT softkey. When this is done, a screen similar to screen [2] is displayed by the VFDT.

Screen [2]

```
DATA   Bits    1 2 3 4 5 6 7 8
BYTE           0 1 1 0 1 0 0 1      <   >  NXT
                                    ■   ■   ■
```

With the two pointer softkeys, the underline can be moved under any one of the 8 bit positions. To change the state from 0 to 1 or 1 to 0, the 1 and 0 keys on the keypad located to the right of the VFDT must be used. By momentarily depressing the NXT softkey in screen [2], screen [1] is displayed with the updated content of the selected byte.

Remarks :

- The entry of the DS0 analyzer pattern instruction from the DS1 Transmit 1 section does not imply that the monitored pattern must be supplied by the 440B. Any pattern IDENTICAL in content to that selected is suitable for bit error detection.
- When carrying-out DS0 transmission performance testing, it is generally desirable to ensure that measurements are not invalidated by the inadvertent change of channel selection of the selection of the pattern. To prevent these changes, it is recommended to use the DS0 protection feature. Instructions for setting-up this feature are given in chapter 3 under MODE menu.

DS0 DATA REAL-TIME BIT DISPLAY

5.4 The momentary depression of the DS0 DATA menu/key located below the VFDT causes the VFDT to display a screen similar to screen [3] below.

Screen [3]

```
DSO Bits :    1 2 3 4 5 6 7 8      RCX #1
              = = = = = = = =      SEL     NXT
                                   ■       ■
```

In screen [3], the average density of ones is displayed for each bit. The headings 1 through 8 indicate the respective bit positions. If a bit is continuously set at state one, a full height stack of horizontal lines is displayed for this bit. If a bit is continuously set at state zero, the stack is empty. If the state of a bit is one 30 % of the time, the stack has about 2 lines (7 lines x 0.33). When monitoring actual DDS data traffic, it is common to have bit 1 through bit 7 represented by a half height stack and bit 8 by a full height stack. When monitoring data test codes, the display consists of a sequence of full and empty stacks as well as the identification of the test code. An example of such a code is given by screen [4].

Screen[4]

```
DSO Bits :          12345678      RCX #1
MUX OUT OF SYNC     00011010      SEL     NXT
                                  ■       ■
```

Table 5.1 below lists the codes identified by the 440B as they are abbreviated on the display.

Code	Description	
X1111110	IDLE CODE	X = solid 1 or solid 0
00101100	DSU LOOPBACK	
00101000	CHAN LOOPBACK	
00101010	OCU LOOPBACK	
00011010	MUX OUT OF SYNC	
00011100	TEST CODE	
00011000	UASGN MUX CHAN	

Table 5.1 Identified DDS Test Codes.

In screens [3] and [4], the #1 identifies that the DS0 channel content is obtained from the DS1 Receiver 1. When the DS0 channel content is to be selected from the DS1 Receiver 2, the SEL softkey must be momentarily depressed. This causes the #1 to be replaced by #2.

DS0 TRANSMISSION PERFORMANCE CHARACTERIZATION

5.5 When equipped with option 05, the DS0 data analyzer compares on a bit-by-bit basis the pattern content in the selected DS0 channel obtained from the DS1 Receiver 1 or 2 with a known pattern. This comparison is the basis for the DS0 transmission performance characterization. The following sections cover the definition of these measurements and how to access them.

DS0 PERFORMANCE INDEX DEFINITIONS

5.5.1 The 440B impairment data processor computes the indices listed in table 5.2. This table provides the definition and the range of values for each index. Additional background information regarding some of these measurements are also included.

Index	Definition	Range
ERR	Bit error count	0 to 9999
BLK ERR	Block error count	0 to 9999
SYNC L-SEC	Synchronization loss-seconds	0 to 9999
BER	Bit error rate	1.0×10^{-3} to
	#Bit ERR's/# bits	0.1×10^{-9}

Table 5.2 Index definitions and ranges

▸ **Bit ERRors**
This counter is active only while pattern synchronization prevails.

▸ **BLK ERRors**
This counter increments by one count for every second in which one or more errors has been detected while pattern synchronization prevails.

▸ **SYNC L-SEC**
This counter increments by one count for each second or fraction of a second during which pattern synchronization is lost.

▸ **BER**
Because the bit error counter is stopped while pattern synchronization is lost, the BER obtained may be more favorable than fact if the number of SYNCH L-SEC is not negligible compared to the duration of the test.

DS0 TRANSMISSION PERFORMANCE MEASUREMENT DISPLAY

5.5.2 By momentarily depressing the DSO DATA menu/key located below the VFDT, you can access the DS0 data measurements performed whether the VFTD displays the DS0 data or not. The first screen of this menu displays the data density histogram and was discussed in section 5.4. When the NXT softkey in screens [3] or [4] is momentarily depressed, a screen similar to screen [5] is displayed by the VFDT.

Screen [5]

PATTERN	ERR	BLK ERR	SYNC L-SEC	#1	
511	314	38	15	PAT	NXT

If pattern synchronization has not been acquired since the most recent RESET, the data fields in screen [5] are each replaced by N/A.

The current pattern selection in screen [5] is automatically updated when the INT DS0 DATA selection in the Transmit #1 is performed. The RCVR selection is indicated by the #1 near the top right hand corner. (If RCVR 2 is selected, this is indicated by #2.)

When depressing the PAT key in screen [5], the next screen [6] is displayed for about 5 seconds.

Screen [6]

To change the test pattern selection	
depress the TRANSMIT DATA key.	NXT

By depressing the NXT softkey in screen [6] prior to the time-out, screen [5] is displayed. When depressing the NXT softkey in screen [5], the VFDT displays a screen similar to screen [7].

Screen [7]

64 kb/s BER	#1
2.2×10^{7}	NXT

If pattern synchronization has not been acquired since the most recent RESET, the data field in screen [7] is replaced by N/A. When depressing the NXT softkey in screen [7], screen [3] is displayed anew.

> **Remark**
> If the 440B is not equipped with option 05, the momentary depression of the NXT softkey in screens [3] or [4] causes the display of screen [8] for a period of 4 seconds.

Screen [8]

PATTERN	BIT ERR	BLK ERR	SYNC L-SEC
Option 05 is not installed			

EXTERNAL DS0 DATA INTERFACE (OPTION 03) DESCRIPTION

5.6 The option 03 provides both a 64 kb/s transmit input interface and a 64kb/s receive output interface. This section describes only the receive output interface; the transmit input interface is described in chapter 10.

When the 440B is equipped with option 03, the content of the DS0 channel selected from either DS1 Receiver 1 or DS1 Receiver 2 is available on the rear panel jack labeled 64 kb/s DATA OUTPUT. At the same time, the 8 kHz clock and the 64 kHz clocks required to analyze the delivered data are supplied on the RECEIVE TIMING SOURCE 5 pin connector.

This set of connectors is suited for attaching a DS0 subrate test set such as the KS-20908 made by WECO or the model 108A made by Telepath Industries.

Additional information regarding the electrical interface is found in chapter 19.

DS0 DATA MEASUREMENT APPLICATION INFORMATION

5.7 The built-in DS0 data measurement capability is particularly useful for trouble sectionalization and for characterizing the data encoding process of a DS0 channel unit. These two applications are discussed below.

DS0 DATA CHANNEL TROUBLE SECTIONALIZATION

5.7.1 When difficulties are encountered in a DS0 data transmission, the trouble is seldom caused by the transmission. Most of the time, the problem is caused by either a defective encoder circuit in the transmitting channel unit or by the decoder circuit in the receiving channel unit. To identify whether the encoder is operating properly, you may test it by following the directions given in the following section. To verify whether the decoder is operating properly, refer to chapter 11.

TRANSMIT DS0 CHANNEL HALF-CHANNEL TESTING

5.7.2 By letting the 440B monitor the DS1 bit stream delivered by a channel bank equipped with a DS0 data channel unit, you can readily determine whether the encoder-half of this channel unit operates properly.

To this end, you need to patch to the DS0 data channel unit input the test pattern generated by a KS 20909 WECO test set (or alternatively a TPI 109A made by Telepath Industries) as shown in figure 5.1 following. Select the desired bit rate as required by the channel unit and send a 511 or a 2047 bit pattern. The 440B DS1 Receiver 1 or 2 PCM input is then patched to the monitor jack of the channel bank transmit circuit. If the DS0 data channel unit operates at 56 kb/s, the 440B can be set to synchronize on the encoded pattern directly and to perform the transmission performance tests described in section 5.5. If the DS0 data channel unit is not operating at 56 kb/s, an auxiliary data test set such as the WECO KS 20908 or the TPI 108A must be attached to the 440B DS0 optional interface port to perform the bit error tests.

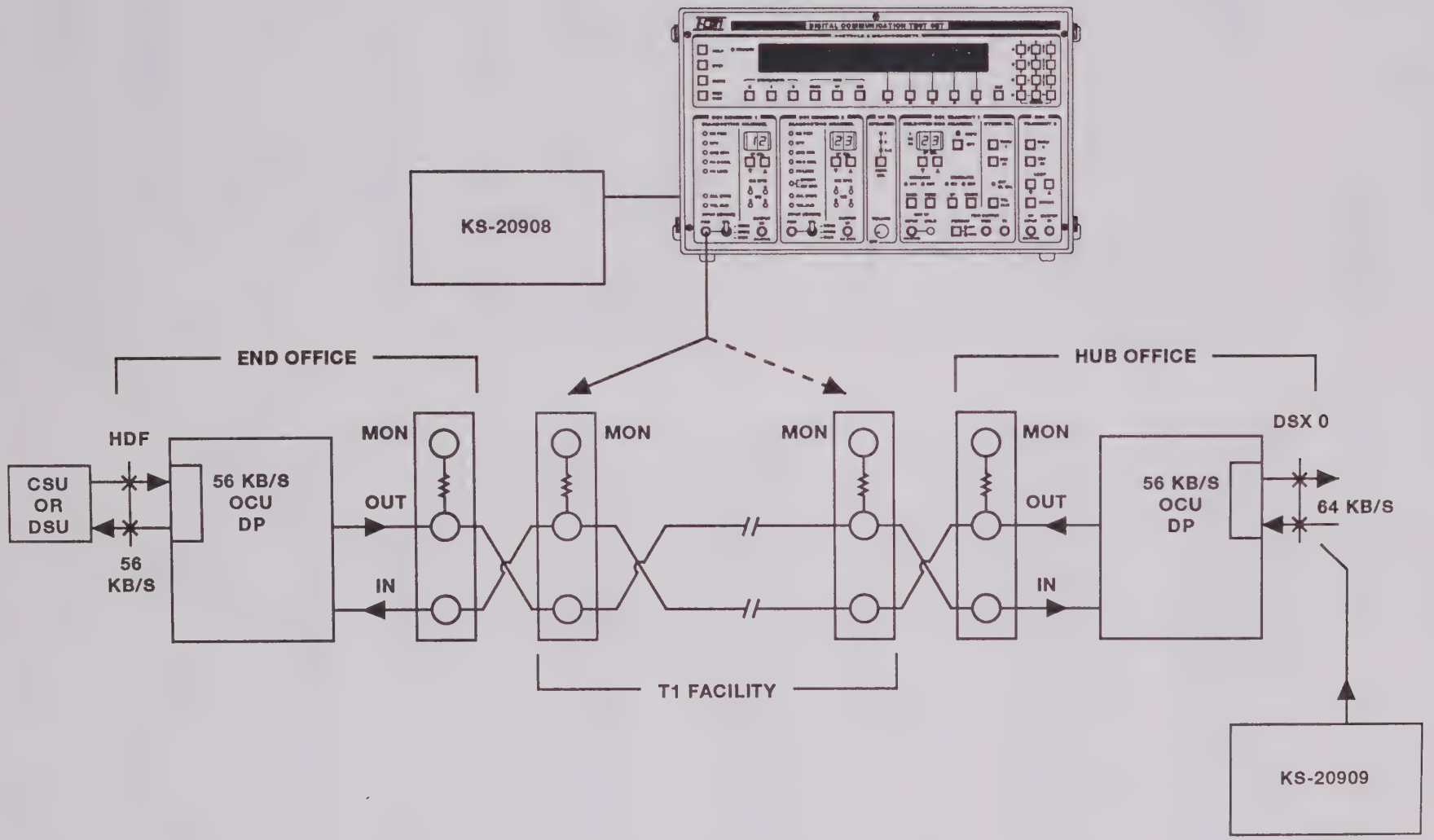


Figure 5-1. Testing A DSO Channel Encoder

6 DS0 CHANNEL VF MEASUREMENTS

INTRODUCTION

6.1 In addition to converting the 64 kb/s content of a selected DS0 channel into a VF signal, each DS1 Receiver delivers a copy of the 64 kb/s stream to a built-in transmission measuring set (TMS). Specialized measurements not performed by this TMS can be made by analyzing the reconstructed VF signal available at the VF OUTPUT jacks in each Receiver section. In this chapter, you will find :

- an overview of the 440B DS0 channel VF measurement capabilities
- directions to set-up the 440B for DS0 VF testing
- general information about each type of VF measurements
- VF half-channel testing application information

DS0 CHANNEL VF MEASUREMENT CAPABILITY OVERVIEW

6.2 The built-in TMS uses a digital signal processor to perform all the VF measurements directly from the selected 64 kb/s bit stream. This technique offers far greater accuracy and stability over time than is possible with the traditional analog based measurements. Moreover, it makes it possible to measure the presence of offset caused by misaligned VF encoder circuits.

The measurements performed by the TMS include :
- RMS level measurement
- tone frequency
- offset
- noise level with C-message filter and 1010 Hz notch filter
- noise level with C-message filter only
- noise level with 35 Hz high-pass filter

All these measurements are readily obtained via the VFDT once the 440B is appropriately set-up.

SETTING-UP THE DS0 CHANNEL VF MEASUREMENT MODE

6.3 To measure the DS0 channel VF parameters, it is necessary for the DS1 Receiver to receive a DS1 formatted bit stream and to let the 440B system format match the format of the monitored DS1 bit stream. In addition, the DS1 Receiver PCM input selection must be set according to the PCM signal source as described in chapter 4. The desired channel is selected on the DS1 Receiver by using either switch located under the channel No. display.

The VF measurements are performed and displayed by calling the DS0 VF menu selected by momentarily depressing the DS0 VF key located below the VFDT. When this key is depressed, a screen similar to screen [1] is displayed by the VFDT.

Screen [1]

VF	dBm0	Hz	Offset	RCX	#1
	-33.5	1277	OK	SEL	NXT

Screen [1] shows the current DS1 Receiver selection (#1). This selection can be changed by momentarily depressing the SEL softkey. Repeated depressions of this key cause the selection to toggle between #1 and #2.

The VF level, the frequency and the offset for the content of the DS0 channel are evaluated and displayed simultaneously. By depressing the NXT softkey in screen [1], a screen similar to screen [2] is displayed.

Screen [2]

VF NOISE (C-MSG w/ 1010 Hz NOTCH)		#1
33.5	dBrnC0	NXT

By depressing the NXT softkey in screen [2], a screen similar to screen [3] is displayed.

Screen [3]

VF NOISE (C-MSG)		#1
33.5	dBrnC0	NXT

When the NXT softkey is depressed in screen [3], screen [4] is obtained.

Screen [4]

VF NOISE (Flat w/35 Hz HP filter)	#1
33.5 dBm0	NXT

When the NXT softkey is depressed in screen [4], screen [1] is displayed again. The loss of framing in the DS1 Receiver from which the DS0 channel VF content is measured causes the value in any of the above screens to be replaced by the message: 'FRAMING LOSS'.

Additional information regarding these measurements are provided in the next section.

VF MEASUREMENT DEFINITIONS

6.4 The measurements given in the sample screens shown in section 6.3 are discussed and clarified in this section.

- VF level measurement
This measurement capability has a range of + 3.2 to -59.9 dBm0. The unit is based on the definition of the dBm (a power of 1 mW dissipated by a 600 Ω resistor corresponds to 0.775 VRMS and is referred to as 0 dBm). When the encoded VF signal is clipped as a result of overload of the encoder, the displayed measurement value reads 'OVERRANGE'. When the encoded VF signal is less than -59.9 dBm0, the measurement value reads '< -60'.

- VF tone frequency measurement
This measurement capability has a range of 50 Hz to 3990 Hz. This range is limited by the 4000 Hz DS0 channel bandwidth. To ensure accuracy of the measurement in the presence of noise, the frequency is only measured when the measured level exceeds -40 dBm0. If this is not the case, the frequency reading is replaced by '****'.

- Offset measurement
This measurement characterizes the algebraic difference over time between the sum of all positive samples and the sum of all negative samples. When this difference divided by the number of samples exceeds 12 counts, the offset reading given by screen [1] is '> 12 counts' otherwise, the offset reads 'OK'. Under normal conditions, this offset is only a few counts on a scale of 8,031 counts.

- Noise level measurements
These measurements are expressed in dBrnC0 if the C-message filter is used or in dBrn0 when only the high pass filter is used. The measurements expressed in dBrn0 differs from the values obtained in dbm0 units by 90 dB; that is

$$\#\ dBrn0 = \#\ dBm0 + 90$$

Automatic compensation is introduced to correct the noise bandwidth lost to the notch when performing C-message + 1010 Hz notch filtered measurements. When the noise level exceeds 93.2 dBrn0/dBrnC0, the displayed value reads OVERRANGE .

ADDITIONAL VF MEASUREMENTS

6.5 Other types of VF measurements can be performed using specialized test instruments to analyze the VF signal delivered by the VF OUTPUT jacks in each DS1 Receiver section. Such measurements include signal distortion, envelop delay distortion, phase jitter, P/AR rating etc.
Each VF output jack delivers a filtered signal precisely reconstructed from the 64 kb/s stream in the selected DS0 channel.

The VF signal level is 0.775 VRMS across a 600 ohm load (0 dBm) when the digital signal delivered by the encoder is 0 dBm0.

DS0 CHANNEL VF MEASUREMENT APPLICATION INFORMATION

6.6 The built-in TMS measurement capability is quite useful for characterizing the encoder circuit performance in a number of equipment : channel banks, transmultiplexers, echo cancellers etc. This section describes the testing of a channel bank transmit half-channel for gain adjustment, gain linearity check, frequency response and idle noise measurements. Additional information is also provided about the offset measurement. The testing approach described here is equally applicable to most other equipment used in PCM systems in general.

TRANSMIT HALF-CHANNEL GAIN ALIGNMENT

6.6.1 The transmit half-channel gain is adjusted by feeding a calibrated signal level to the input of a channel unit and measuring the encoded level directly from the PCM bit stream as illustrated in figure 6.1.

Normally, the measurement is performed at a frequency of 1004 Hz. Care must be taken for that frequency not to be precisely 1000 Hz as this might cause erratic level readings due to the 8000 Hz sampling frequency used in the channel bank. The amplitude of the VF signal applied to the channel unit under test should be set to the value specified by the manufacturer or the company practices. Typically, this level is set to let the VF to digital encoder yield 0dBm0 to the DS0 channel.

The gain is aligned by adjusting the transmit gain to read 0.0 dBm0 (or another recommended value) on the 440B.

TRANSMIT HALF-CHANNEL GAIN LINEARITY CHECK

6.6.2 The gain linearity check consists in comparing the set of measurements obtained by measuring the DS0 channel content delivered by the encoder under test with the set of signal level values sequentially applied to the channel unit VF input.

By plotting the set of input levels on one axis and plotting the set of values read on the 440B on the other axis of a rectangular coordinate system, all deviations from a line inclined by 45° illustrate the gain non-linearity for the transmit half-channel.

TRANSMIT HALF-CHANNEL FREQUENCY RESPONSE CHECK

6.6.3 To perform this test, refer to the set-up illustrated in figure 6.1. The frequency response of the transmit half channel is obtained by plotting on a graph the level measured by the 440B TMS for each frequency of the signal applied to the channel unit VF input.

To ensure accurate results, care must be taken to keep the signal level applied to the VF input constant during the test. The resolution of the frequency response is increased by reducing the size of the frequency steps. This results in taking more measurements and requires more time.

TRANSMIT HALF-CHANNEL IDLE NOISE MEASUREMENT

6.6.4 Using still the set-up illustrated figure 6.1, you can measure the transmit half-channel idle noise by setting the 440B to measure the desired type of noise and providing a quiet termination to the channel unit VF input port.

The obtained TMS noise reading requires no correction or interpretation and can be used readily as a measure of the noise contributed by the transmit-half portion of the DS0 channel. Typically, this transmit half contributes the most to the overall idle channel noise.

TRANSMIT HALF-CHANNEL OFFSET

6.6.5 Offset found in a DS0 channel is almost invariably contributed by either an out-of-calibration or a defective VF filter/encoder circuit. The presence of offset is known to cause out-of-specification signal distortion and gain non-linearity. In addition, the operation of some echo canceller malfunctions have been traced to excessive amounts of offset.

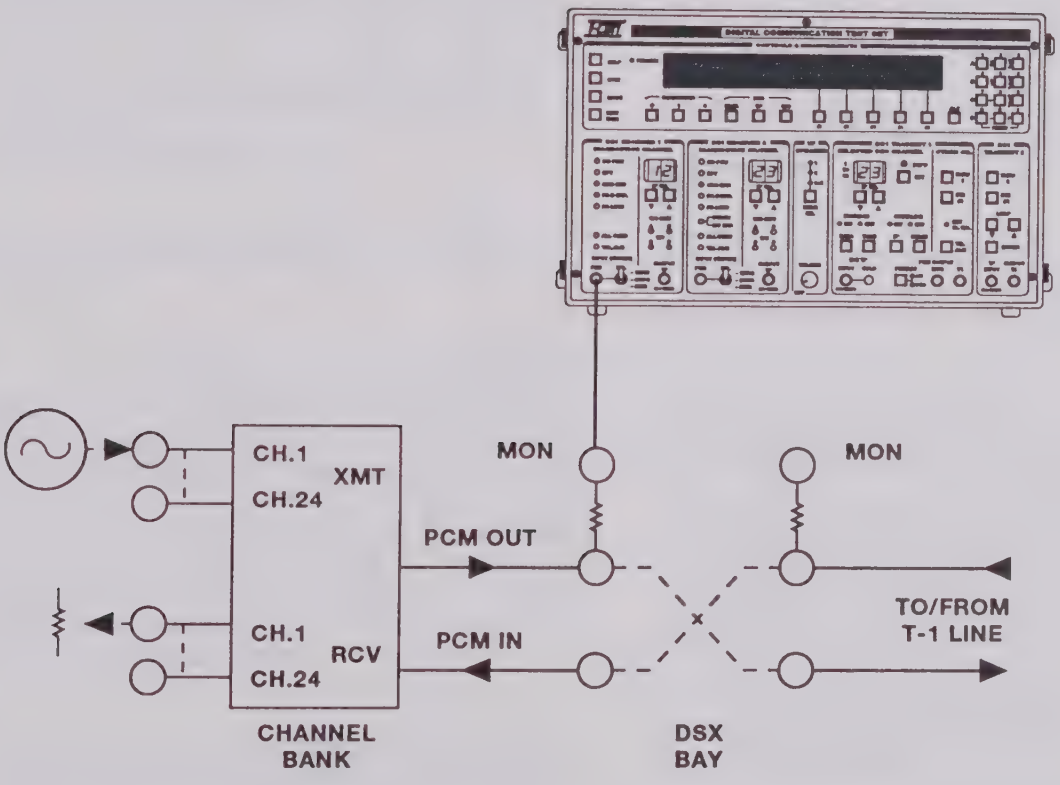


Figure 6-1. Transmit Half-Channel Gain Alignment

7. DS0 CHANNEL SIGNALING STATE DISPLAY & MEASUREMENTS

INTRODUCTION

7.1 A number of useful supervision monitoring features are built-in the 440B and when necessary, optional supervision measurement capabilities can be added to the instrument. In this chapter you will find :

- a description the 440B DS0 supervision monitoring features
- a description of the wink measurement capability
- directions to set-up the 440B for wink parameter measurement
- supervision related information

DS0 SUPERVISION MONITORING FEATURE DESCRIPTION

7.2 In addition to reconstructing the VF signal from the 64 kb/s stream contained in the selected DS0 channel, each DS1 Receiver decodes the states of the signaling bits (channel supervision) and displays those states in real-time with bi-color LED's. The states of the signaling bits (A, B, C and D in an ESF formatted bit stream, A and B in an SF formatted bit stream) are displayed whenever framing prevails in a DS1 Receiver. The state 1 is displayed by the color red and state 0 by the color green.

Notes

- If the 440B is equipped with option 05 and the DS1 Receiver 2 synchronizes on the monitored pattern (SYNC LED is lit) all signaling LED's in this section are turned off.

- when it is desired to record signaling bit activity over time, the electrical outputs associated with the four signaling LED's in each DS1 Receiver, available on the rear panel 9-pin connector (J19) can be used as input by a strip chart recorder. Additional information on this connector is found in chapter 19.

Independently of the LED display, the VFDT can display the state of the signaling bits for the 24 DS0 channels in each of the bit streams monitored by the DS1 Receiver 1 and 2 simultaneously. To have the VFDT display these states, first select the SIG menu by momentarily depressing the DSO SIG key located below the VFDT. This causes the VFDT to display a screen similar to screen [1].

Screen [1]

```
SIGNALING:    BITS   MF   DTMF        DP   WINK
                                       <    >   ENTR
                                       ■    ■   ■
```

The current selection is underlined. By momentarily depressing either pointer softkey, let the BITS heading be underlined and depress the ENTR softkey. This last entry results in displaying a screen similar to screen [2].

Screen [2]

```
A1/B1 %%%% %%%% %%%% %%%% %%%% %%%%   ALT
A2/B2 %%%% %%%% %%%% %%%% %%%% %%%%   SEL
                                       ■
```

Screen [2] shows on the top line the state of the A and B signaling bits for the bit stream monitored by the DS1 Receiver 1. The bottom line shows the corresponding states for the 24 channels in the bit stream monitored by the DS1 Receiver 2. In each line the states of the signaling bits A are on top and B on the bottom. The leftmost column corresponds to channel 1 and the rightmost to channel 24.

If framing is lost on either line, the state of the signaling bits for this line is replaced by the message: 'FRAMING LOSS'.

If the current system format selection is SLC-96, D1D, D2 or D3/D4, the momentary depression of the ALT SEL softkey in screen [2] yields screen [1] again. If instead, the current system selection is ESF, the momentary depression of the ALT SEL softkey yields a screen similar to screen [3].

Screen [3]

```
A1/B1 %%%% %%%% %%%% %%%% %%%%        ALT
C1/D1 %%%% %%%% %%%% %%%% %%%%        SEL
                                       ■
```

This screen displays the signaling states for the A, B, C & D bits in the 24 channels of the bit stream monitored by the DS1 Receiver 1. The depression of

The softkey in screen [3] yields a screen similar to screen [4].

Screen [4]

```
A2/B2 %%%% %%%% %%%% %%%% %%%%        ALT
C2/D2 %%%% %%%% %%%% %%%% %%%%        SEL
                                          ■
```

This screen displays the signaling states for the A, B, C & D bits in the 24 channels of the bit stream monitored by the DS1 Receiver 2. The depression of the softkey in screen [4] yields a screen similar to screen [5].

Screen [5]

```
C1/D1 %%%% %%%% %%%% %%%% %%%%        ALT
C2/D2 %%%% %%%% %%%% %%%% %%%%        SEL
                                          ■
```

The upper line shows the signaling states for the C & D bits in the 24 channels of the bit stream monitored by the DS1 Receiver 1. The lower line shows the signaling states for the C & D bits in the 24 channels of the bit stream monitored by the DS1 Receiver 2. The depression of the softkey in screen [5] yields screen [1] again.

NOTES:

A rear panel selection switch allows you to choose the symbols used for representing the signaling states. When the switch S4 position 7 is set to ON, the signaling state is shown as a 1 for state one and 0 for state zero. When the switch S4 position 7 is set to OFF, the signaling state is shown as "." for state one and ■ for state zero. This representation is somewhat easier to read from a distance.

Because the VFDT refreshing rate is approximately 10 refreshes per second, changes in states at this rate or higher may not be displayed. This is particularly true for winks. Fortunately, the optional wink measurement capability more than makes up for this limitation.

WINK MEASUREMENT CAPABILITY DESCRIPTION

7.3 When the 440B is equipped with option 06, you can obtain the measure of single wink as well as multiple wink duration and delay. The wink, or momentary off-hook condition, is sent by the called office using the supervision bits.

The wink duration is measured as the time interval between the on-hook/off-hook transition and the off-hook/on-hook transition of the wink. Wink delay is measured as the time elapsed between the onset of the channel seizure and the off-hook/on-hook wink transitions.

Winks are expected and measured only when occurring on the bit stream monitored by the DS1 Receiver 2. Consequently, channel seizure is expected on the bit stream monitored by the DS1 Receiver 1 or the bit stream delivered by the DS1 Transmit 1.

The 440B has the ability to measure wink duration and delay for up to three consecutive winks. This is designed to handle the measurement of the winks associated with feature group D signaling.

The set-up required to measure the wink parameters is described in the next section.

SETTING-UP THE 440B FOR WINK PARAMETER MEASUREMENT

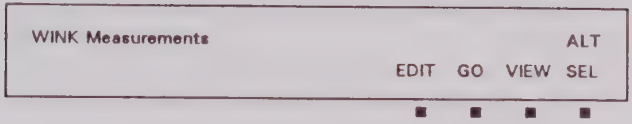
7.4 The sequence of screens starting with screen [1] below illustrates how the 440B must be set-up for performing wink parameter measurements.

Screen [1]

```
SIGNALING:    BITS   MF   DTMF      DP   WINK
                                     <    >   ENTR
                                     ■    ■    ■
```

By momentarily depressing either pointer softkey in screen [1], let the WINK heading be underlined and depress the ENTR softkey. This last entry results in displaying screen [6].

Screen [6]

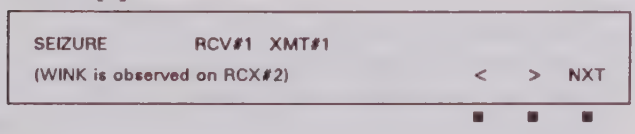


The depression of the ALT SEL softkey in screen [6] causes the VFDT to display screen [1] again. The VIEW softkey is used to display the acquired measurements. The GO softkey is used to initiate the measurement. The EDIT softkey is used to specify the following conditions :

- whether the seizure is to be observed from the DS1 Receiver 1 or from the DS1 Transmit 1,
- the state of the bit identifying the line seizure and
- the bit identifying the wink.

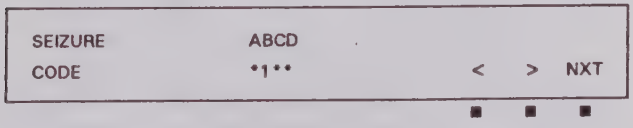
Depressing the EDIT softkey yields a screen similar to screen [7].

Screen [7]



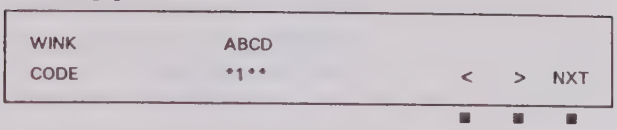
The underline [not shown] in screen [4] can be placed under the XMT#1 or RCX#1 headings by using either pointer softkeys. When the NXT softkey in screen [7] is depressed, a screen similar to screen [8] is displayed. The selection shown in this screen indicates that bit B only is material and the state of this bit is to be 1 to indicate seizure. The state is set by using the 0, 1 and * keys in the keypad. The * stands for the "don't care" state. A legitimate entry requires that one and only one bit be given a defined state. The C and D bits are shown whether the system format is ESF or not.

Screen [8]



The depression of the NXT softkey in screen [8] causes a screen similar to screen [9] to be displayed by the VFDT. This screen has essentially the same requirements as screen [8].

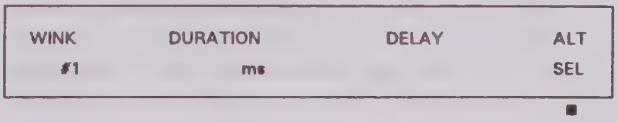
Screen [9]



The wink code is the off-hook state reduced to a single significant bit state. When the NXT softkey in screen [9] is depressed, screen [6] is displayed again. From this point on, all wink measurements will be based on the newly entered states. These states are stored as battery powered RAM and thus do not need to be re-entered after the 440B power is turned off.

Depressing the GO softkey in screen [6] results in clearing away any previously acquired measurement and to display screen [10] until the measurements are made. When the measurements are

Screen [10]



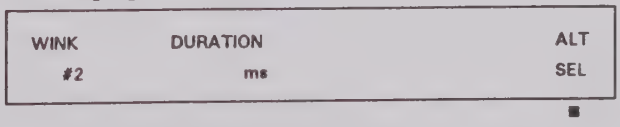
obtained, they are displayed as shown in screen [11].

Screen [11]

If a value exceeds 1000 ms, the display for that measurement reads >1000. If in screens [10] or [11] the ALT SEL softkey is depressed, screen [1] is displayed anew.

If in screen [11] the NXT softkey is pressed, screen [12] is displayed until the second wink measurement is completed.

Screen [12]



When the second wink measurement has been detected, screen [13] as an example, is displayed.

Screen [13]

WINK	DURATION	ALT
#2	120 ms	NXT SEL

If in screen [13] the NXT softkey is pressed, screen [14] is displayed until the third wink measurement is completed.

Screen [14]

WINK	DURATION	ALT
#3	ms	SEL

When the third wink measurement has been detected, the value is displayed as in other screens. If in screen [14] the ALT SEL softkey is depressed, screen [6] is displayed anew.

If in screen [3] the VIEW softkey is depressed, all previously acquired wink related measurement values are preserved and screen [10] is displayed. From this point onward, the opera-tion is the same as if the screen [10] had been accessed by pressing the GO softkey in screen [6].

Remarks :

- If more than 3 winks take place, only the first three are measured, all others are discarded.
- Because the wink measurements are obtained by accessing a DS0 channel, a change in the channel No. selection disrupts the acquisition.
- The wink measurements do not require that the VFDT display any wink measurement related screen. A measurement can be performed in the background mode and displayed later.
- Wink delay is measured only for the wink #1.
- If entry in the WINK menu is attempted in a 440B not equipped with option 06, the following screen is displayed during 4 seconds following the unsuccessful attempt.

Option 06 must be installed to obtain wink measurements

DS0 SUPERVISION MONITORING APPLICATION INFORMATION

7.5 The monitoring of the supervision simultaneously in all the 24 DS0 channels in the two transmission directions of DS1 system has several applications. The three most popular are :

- Detection of idle channels. This is useful to identify which channel can be selected for drop-and-insert testing or to subjectively gauge the traffic on a DS1 line.
- Detection of non-functional channels. These channels are either permanently busy or idle or exhibit a signaling bit state inconsistent with the convention for the channel unit type used in the time slot.
- Detection of problem conditions affecting several channels. The simultaneous change of signaling states in several channels provides a useful clue to the origin of the fault.

For reference, a summary of the signaling state assignments for the most commonly used types of channel units is given in table 7.1 and table 7.2 in the following pages.

CHANNEL UNIT TYPE	E&M SIGNALING CIRCUIT CONDITION TO PLR CHANNEL	TRANSMIT @ A	TRANSMIT @ B	RECEIVE @ A	RECEIVE @ B	PLR CHANNEL UNIT CONDITION TO E&M SIGNALING CIRCUIT
PULSE LINK	E LEAD OPENED	0	0	*	*	*
REPEATER	E LEAD GROUNDED OR LOOPED (1)	1	1	*	*	*
(PLR)	*	*	*	0	*	M LEAD GROUNDED IR IOEB (1)
4W, 600Ω	*	*	*	1	*	M LEAD BATTERY OR LOOPED

* Either State or Condition.

(1) Option Selected by screw switch

@ A and B Signaling Channel States are shown as they exist on the T1 line.

CHANNEL UNIT TYPE	OFFICE CONDITION TO CHANNEL UNIT	TRANSMIT @ A	TRANSMIT @ B	RECEIVE @ A	RECEIVE @ B	CHANNEL UNIT CONDITION TO OFFICE
DPO	LOOP OPEN	0	0	*	*	*
XMT	LOOP CLOSURE	1	1	*	*	*
	*	*	*	0	*	NORMAL BATTERY
RCV	*	*	*	1	*	REVERSE BATTERY
DPT	NORMAL BATTERY	0	0	*	*	*
XMT	REVERSE BATTERY	1	1	*	*	*
	*	*	*	0	*	LOOP OPEN
RCV	*	*	*	1	*	LOOP CLOSURE
4WE&M	M-LEAD GROUNDED OR OPEN	0	0	*	*	*
XMT	M-LEAD BATTERY	1	1	*	*	*
2WE&M	*	*	*	0	*	E-LEAD OPEN
RCV	*	*	*	1	*	E-LEAD GROUNDED OR LOOPED
RPO	LOOP OPEN	0	0	*	*	*
XMT	LOOP CLOSURE	1	1	*	*	*
	*	*	*	0	1	NORMAL BATTERY NO REVERTIVE PULSE
RCV	*	*	*	0	0	NORMAL BATTERY REVERTIVE PULSE
	*	*	*	1	*	REVERSE BATTERY NO REVERTIVE PULSE
RPT	NORMAL BATTERY NO REVERTIVE PULSE	0	1	*	*	*
	NORMAL BATTERY REVERTIVE PULSE	0	0	*	*	*
XMT	REVERSE BATTERY	1	0	*	*	*
	*	*	*	0	0	LOOP OPEN
RCV	*	*	*	1	1	LOOP CLOSURE
	*	*	*	0	1	NOT ALLOWED
	*	*	*	1	0	NOT ALLOWED
SDPO	LOOP OPEN	0	0	*	*	NO SLEEVE GROUND **
XMT	LOOP CLOSURE	1	1	*	*	SLEEVE GROUND **
	*	*	*	0	*	NORMAL BATTERY
RCV	*	*	*	1	*	REVERSE BATTERY

@ A and B Signaling Channel States are shown as they exist on the T1 line.

* Any state or condition.

** Either normal or reverse battery.

Table 7.1 Channel Unit Signaling State Assignment

CHANNEL UNIT TYPE	OFFICE CONDITION TO CHANNEL UNIT	TRANSMIT @ A	TRANSMIT @ B	RECEIVE @ A	RECEIVE @ B	CHANNEL UNIT CONDITION TO OFFICE
FXO	NO TIP GROUND, NO RINGING	1	1	*	*	*
	TIP GROUND, NO RINGING	0	1	*	*	*
XMT	TIP GROUND, RINGING	0	0	*	*	*
	NO TIP GROUND, RINGING||||||||||||||||	?	?	*	0	(RING GROUND)||||||||||||||||||||
	NO TIP GROUND, RINGING||||||||||||||||	?	0	*	1	(NO RING GROUND)|||||||||||||||||
	*	*	*	0	1	LOOP OPEN, NO RING GROUND
	(TIP GROUND)	0	*	0	0	LOOP OPEN, NO RING GROUND
	(NO TIP GROUND)	1	*	0	0	LOOP OPEN, RING GROUND
RCV-	*	*	*	1	1	LOOP CLOSURE, NO RING GROUND
	(TIP GROUND)||||||||||||||||||||||||||	0	*	1	0	LOOP CLOSURE, NO RING GROUND||
	(NO TIP GROUND)||||||||||||||||||||||||||	1	*	1	0	LOOP OPEN, RING GROUND|||||||||

CHANNEL UNIT TYPE	STATION OR PBX CONDITION TO CHANNEL UNIT	TRANSMIT @ A	TRANSMIT @ B	RECEIVE @ A	RECEIVE @ B	CHANNEL UNIT CONDITION TO STATION OR PBX
FXS	LOOP OPEN, NO RING GROUND	0	1	*	*	*
	LOOP OPEN, RING GROUND||||||||||||||||	0	1	0	*	(TIP GROUND)||||||||||||||||||||
	LOOP OPEN, RING GROUND	0	0	1	*	(NO TIP GROUND)
XMT	LOOP CLOSURE, NO RING GROUND|||||||	0	1	1	*	(NO TIP GROUND)||||||||||||||||||
	LOOP CLOSURE, NO RING GROUND	1	1	0	*	(TIP GROUND)
	LOOP CLOSURE, RING GROUND||||||||||	1	1	0	*	(TIP GROUND)||||||||||||||||||||
	LOOP CLOSURE, RING GROUND||||||||||	0	0	1	*	(NO TIP GROUND)||||||||||||||||||
	*	0	*	1	*	NO TIP GROUND, NO RINGING
RCV	*	*	1	0	1	TIP GROUND, NO RINGING
	(LOOP CLOSURE)	1	1	0	0	TIP GROUND, NO RINGING
	(LOOP OPEN)	0	1	0	0	TIP GROUND, RINGING

@ A and B signaling channel states are shown as they exist on the T1 line.

* Any state or condition.

? Indeterminate/

||| Abnormal condition with no application.

( ) Condition existing at distant end of VF connection for receiver.

( ) Condition existing at distant end of overall connection for transmitter.

Table 7.2 Channel Unit Signaling State Assignment

8. DS0 CHANNEL TELEPHONE NUMBER DISPLAY & ANALYSIS

INTRODUCTION

8.1 The DS0 data, VF and supervision monitoring and measurement capability built-in the 440B can be optionally augmented to include the decoding, the capture and the display of MF, DTMF and DP encoded telephone numbers. In this chapter you will find :

- a description the 440B telephone number decoding and display capabilities
- directions to set-up the 440B for decoding/capturing telephone numbers
- directions for displaying the captured telephone numbers

If the 440B is not equipped with option 06, the content of this chapter is not directly applicable to the operation of the instrument.

TELEPHONE No. CAPTURE AND DISPLAY CAPABILITY DESCRIPTION

8.2 When equipped with option 06, the 440B can decode telephone numbers encoded with either MF (multi-frequency tones), DTMF (dual-tone multi-frequency) or DP (dial pulses). The digit decoder analyzes the tone and pulse encoded numbers using digital signal processing techniques to obtain highly accurate and repeatable results.

You may set the telephone number decoder (TND) to monitor the content of the selected DS0 channel either from Receiver 1 or 2 and to identify selectively those tone combinations or signaling bit sequences consistent with the codes used for transmitting telephone numbers. Whenever the TND is set to identify MF or DTMF encoded numbers, each occurrence of a legitimate tone combination results in the storage of the corresponding digit or symbol in a 40-digit buffer. Likewise, whenever the TND is set to identify DP encoded numbers, each occurrence of a legitimate sequence of signaling states results in the storage of the corresponding digit in the 40-digit buffer.

A string of up to 40 digits and symbols can be stored in the buffer. Each decoded digit or symbol is entered into the buffer in the order received until the buffer is full. To ensure maximum use of the buffer space, pauses between digits or groups of digits are not displayed. Whenever the buffer is full, any additional symbol or digit is discarded. In other words, the buffer always contains the first 40 digits captured since initialization. Of course the actual number of digits captured and stored in the buffer may be less than 40.

The decoding/capture capability is completely distinct from the display system. As a result, in the 440B, you may be displaying parameters unrelated to signaling while the TND identifies and stores a telephone number. The next paragraph describes how to set-up the telephone number decoding and capture capability.

SETTING-UP THE TND FOR CAPTURE OF TELEPHONE NUMBERS

8.3 To acquire a telephone number from a monitored bit stream, the user must first set the telephone number decoder as required by selecting the coding type from the DS0 SIG menu. The DS0 SIG menu is displayed by the vacuum fluorescent display tube (VFDT) when the DS0 SIG key in the Control and Measurements section is momentarily depressed. This menu is illustrated by screen [3] on folowing page.

Screen [3]

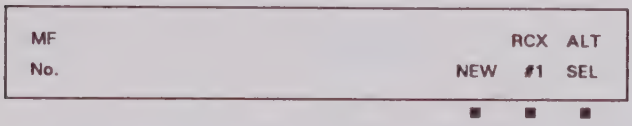
SIGNALING :	BITS	MF	DTMF	DP	WINK
				<	> ENTR
				■	■ ■

If, upon depressing the DS0 SIG key another screen is displayed instead, a second momentary depression of the DS0 SIG key yields the menu screen [3]. The code selection is obtained by placing the underline (not shown) under the MF, DTMF or DP headers and depressing the ENTR softkey. The underline is moved right or left by momentarily depressing the pointer softkeys.

If the MF header is underlined when the ENTR key is depressed in screen [3], the TND is poised to decode and capture MF encoded telephone numbers. The depression of the ENTR key in screen [3] is also accompanied by the display of a screen similar to

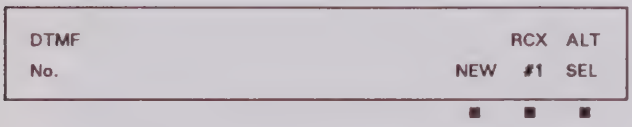
screen [4] below. Screen [4] illustrates an empty MF buffer.

Screen [4]



If the DTMF header is underlined when the ENTR key is depressed in screen [3], the TND is poised to decode and capture DTMF encoded telephone numbers. The depression of the ENTR key in screen [3] is also accompanied by the display of a screen similar to screen [5] below. Screen [5] illustrates an empty DTMF buffer.

Screen [5]



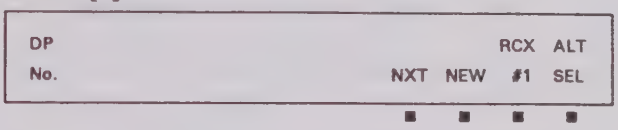
The momentary depression of the NEW softkey in screens [4] and [5] is required only when you need to clear the buffer. (The buffer is cleared automatically when the encoding mode is changed in the DS0 SIG menu.) The momentary depression of the RCX softkey causes the selection to toggle between #1 and #2 to select the Receiver 1 or 2. The depression of the ALT SEL softkey causes the VFDT to display the menu in screen [3].

If the DP header is underlined when the ENTR key is depressed in screen [3], the TND is poised to decode and capture DP encoded telephone numbers. At the same time, screen [6] is displayed by the VFDT to let you check, and change when desired, the on-hook (↓) and off-hook (↑) states used for the detection of the DP encoded telephone numbers.

Screen [6]

When the VFDT displays screen [6], you may change the default states shown by entering the desired 1/0 codes using the numeric keypad and the pointer softkeys. These softkeys allow you to place the underline (not shown) under the desired position. If the selection is as desired, the momentary depression of the NXT softkey in screen [6] is accompanied by the display of a screen similar to screen [7] below. Screen [7] illustrates an empty DP buffer.

Screen [7]



By pressing the ALT SEL softkey in screen [7], screen [3] is displayed anew. The RCX selection (#1) operates in the same manner as described in screen [4] or [5]. From this point on, the TND is ready to capture any DP encoded telephone number as specified whether the screen [7] is displayed or not.

The momentary depression of the NEW softkey in screens [7] is required only if you need to clear the buffer. (The buffer is cleared automatically when the encoding mode is changed in the DS0 SIG menu.) The momentary depression of the RCX softkey causes the selection to toggle between #1 and #2 to select the Receiver 1 or 2. The depression of the ALT SEL softkey causes the VFDT to display the menu in screen [3].

Remarks

- The capture of a telephone number in a DS1 bit stream always requires that the DS1 Receiver monitoring the line be framed. Failure to acquire framing prevents the decoding of telephone numbers.

- Because the telephone number is obtained by accessing a DS0 channel, changes in the channel No. selection disrupt the acquisition process.

The next paragraph covers the set-up of the 440B to display the content of the TND buffer.

SETTING-UP THE 440B TO DISPLAY THE TELEPHONE NUMBERS

8.4 The 440B can display all the MF, DTMF and DP encoded digits and symbols monitored in the selected DS0 channel. The list of these digits and symbols is given in table 8.1 on the next page.

Coding	Digits/Symbols
MF	0-9, KP, ST, ST1, ST2P, ST3P
DTMF	0-9, A, B, C, D
DP	0-9

Table 8.1

Note:
The symbols used for representing the MF KP and ST signals are as follows:

KP : [,
ST :],
ST1P : -,
ST2P : =,
ST3P : ≡

The display of the captured digits and symbols may take place during the capture or at any time later, at your convenience. If the display is to take place upon capture, it is only required not to depress the ALT SEL key in screens [4], [5] or [7]. By letting the VFDT display these screens, each newly captured digit is displayed upon detection and added to the content of the buffer as long as the content does not exceed 40 digits or symbols.

The display of the captured digits and symbols may also take place at any other time. When you wish to display the content of the TND buffer, you need only momentarily depress the DS0 SIG key in the Control and Measurements section. This entry causes the VFDT to display the screen in the DS0 SIG menu from which the exit was made. For instance, if after setting the detection parameters for a DP encoded number with screen [7], you exited the DS0 SIG menu, upon depressing the DS0 SIG key, the VFDT displays again screen [7]. If a (DP encoded) telephone number was captured and stored in the buffer, then screen [7] is replaced by a screen similar to screen [8].

Screen [8]

```
DP    12345678901234561234567                    RCX  ALT
No.   890123456                    NXT  NEW   #2   SEL
                                   ■    ■     ■    ■
```

The measurement of pulse repetition rate and percent break which accompanies the capture of DP encoded telephone numbers can be displayed by momentarily depressing the NXT softkey in screen [8]. An example of a typical measurement is given by screen [9].

Screen [9]

```
DP AVG PPS        AVG      BREAK     [#2]     ALT
    10.3        61.4%                         SEL
                                              ■
```

The [#2] in screen [9] indicates that the measurement was performed on the bit stream monitored by the DS1 Receiver 2.

Remarks :

- To obtain an accurate measurement of the average pulse repetition rate (PPS) and of the percentage break requires that a minimum of 5 digits, each with value greater than 1 are received. Until this is the case, the values displayed for the PPS reading and the AVG BREAK are .0 and .0% respectively.

- When a DP encoded digit is unrecognized or contains a glitch the character E replaces the mangled digit.

The depression of the ALT SEL softkey in screen [9] causes the DS0 SIG menu (screen [3]) to be displayed anew.

If the TND was set for MF or DTMF coded telephone numbers, the process is the same as for DP coded numbers. However, in this case, no measurement of PPS or % BREAK is provided.

MISCELLANEOUS INFORMATION

8.5 Tables 7.1 and 7.2 in chapter 7 provide a handy reference for the on-hook and off-hook signaling states required by a variety of channel units commonly used in digital channel banks. You may want to refer to these tables when you have to change the signaling states as provided for by screen [6] above.

It should be noted that the newly entered signaling states specifying the on-hook and off-hook conditions are stored upon entry in screen [6] into a battery protected RAM. As a result, this data does not vanish when the 440B power is turned off.

9. DS0 CHANNEL AUDIO MONITORING

INTRODUCTION

9.1 The DS0 channel audio monitoring capability provides a very useful addition to the 440B's other built-in means of evaluating the content of the selected DS0 channel. In this chapter you will find :

- a description the VF Speaker section capabilities
- directions to operate the controls in this section
- application related information

VF SPEAKER SECTION CAPABILITY DESCRIPTION

9.2 When monitoring a DS1 bit stream, each DS1 receiver performs the (Mu-law) decoding of the content of a selected DS0 channel. The reconstructed, band-limited signal is available at the VF output port in each DS1 Receiver section. At the same time, a copy of each VF signals is delivered to a selector/mixer and a VF amplifier controlled by the VF Speaker section.

The selector/mixer allows you to select either VF signal separately or to mix them together. The signal delivered by the selector/mixer is amplified and sent to a speaker located on the rear panel of the instrument. The VF amplifier gain is adjustable over a wide range to provide for the comfortable listening of weak and strong signals alike.

In summary, this section allows you to selectively listen to the decoded signal in a channel monitored from either or both DS1 lines and to perform a subjective evaluation of the signal.

OPERATION

9.3 The selection of the VF source is displayed by the lit LED associated with the SEL key. Each momentary depression of the key causes the selection to change to the next logical one in the sequence.

The VF amplifier gain can be adjusted by setting the volume control knob as desired. When set fully counterclockwise, the gain is minimal and the speaker is silent.

One should be mindful of the fact that the VF delivered by each DS1 Receiver is automatically squelched when framing is lost by the receiver from which the VF signal is monitored.

APPLICATIONS

9.4 The applications for the capabilities afforded by the VF Speaker section fall into two categories: signal identification and subjective testing of the transmission quality.

Signal ID

When tracking a channel through a DACS or a digital switch, it is often convenient to insert a tone in a DS0 channel carried by one DS1 bit stream and to track this channel in another DS1 bit stream by listening for the tone while changing the DS0 channel number selection. Additionally, the VF speaker allows you to readily identify the nature of the signal carried by a DS0 channel since voice and data yield substantially different sounds.

Subjective Testing

By selectively monitoring either side or both sides of a call in progress a trained operator can often quickly determine whether the channel meets the noise objective or the nature of the interference if any. For instance the presence of echoes, low trans-hybrid loss, signal distortion and noise is readily identifiable by simply listening to the DS0 channel.

10. DS0 CHANNEL DATA SIMULATION

INTRODUCTION

10.1 The 440B DSO channel monitoring and measuring capabilities, is complemented with a very versatile DS0 channel simulator. This simulator, embedded in the DS1 Transmit 1 section, encompasses the full range of signals one is likely to need to characterize the transmission of a DS0 channel: data, tones/VF, supervision as well as telephone numbers encoded in several ways. These signals may be provided either by built-in sources or by external ones. This chapter concentrates on the optional DS0 data sending capabilities and includes :

- a description the DS0 data simulation capability
- directions for operating the DS0 data sending capability
- application information

If the 440B is not equipped with option 03 or 05, the content of this chapter is not directly applicable to the operation of the instrument.

DSO DATA SIMULATION CAPABILITY DESCRIPTION

10.2 When the 440B is equipped with options 03 and 05, two basic choices are offered when the selected DS0 channel in the DS1 Transmit 1 is to contain data: a selection of internal 56/64 kb/s data signals or the use of externally supplied data signals.

If the 440B is equipped only with option 03, the DS0 channel can only send the data externally supplied. Conversely, if the 440B is equipped only with option 05, the DS0 channel can only send the data generated internally by the 440B.

The selection of internal data signals include the quasi-random codes 511 (2^9-1) and 2047 (2^{11}-1) as well as an 8-bit user selectable pattern. In this case, the same 8-bit byte is repeated 8000 times per second, yielding 64 kb/s. This last feature allows you to create various stress patterns as well as to duplicate some of the codes used when testing the DDS network.

The selection of externally supplied 64 kb/s data stream requires that the 440B be equipped with option 03. This option provides an interface between the 440B and data test sets commonly used to service the DDS network such as the WECO KS20909 and the Telepath Industries TPI 109A. In addition to the patterns discussed above, these sets can supply the DS0A subrate test patterns.

When an attempt is made to use the internally generated patterns when the option 05 is not installed in the 440B, the VFDT displays the following screen [1].

Screen [1]

```
Option 05 must be installed to select
internally generated 64 kb/s patterns
```

The next paragraph provides set-up information.

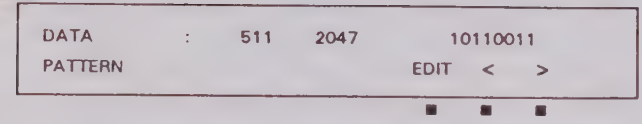
SETTING-UP THE DS0 DATA SENDING CAPABILITY

10.3 The DS1 Transmit 1 section is the only one capable of sending data in a DS0 channel. When the DS1 Transmit 1 section is operated in the stand alone mode, the selected DS0 channel contains DATA whenever the DATA key/LED is either steadily lit or in the FLOSO state. When the DS1 Transmit 1 section is operated in the THRU mode, the DSO channel selection is active only if the SET key/LED is not lit. If lit, the selection can be activated by the momentary depression of the SET key.

When depressing the DATA key, the FLOSO state is transferred to this key and the screen displayed by the VFDT depends on the configuration of the 440B and on whether a plug is inserted in the DS0 interface DATA INPUT jack.

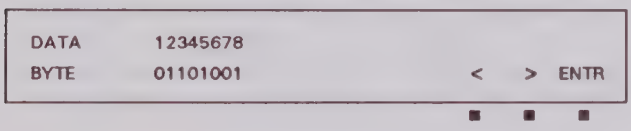
When the 440B is equipped with option 05 and a plug is not inserted in the option 03 64 kb/s DATA INPUT jack, the momentary depression of the DATA key causes the VFDT to display a screen similar to screen [2] below.

Screen [2]



In screen [2], one of the headings is underlined (not shown). The EDIT header appears only when the 8-bit byte is underlined. The underlined data pattern is supplied to the selected DS0 channel. The data pattern selection can be changed by momentarily depressing either arrow softkey. Whenever desired, you may change the content of the 8-bit byte by momentarily depressing the EDIT softkey. When this is done, a screen similar to screen [3] is displayed by the VFDT.

Screen [3]

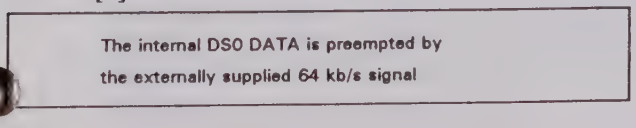


Screen [3] enables you to replace the currently displayed combination of 1 and 0 by any other arbitrary combination by using the 1 and 0 keys in the numeric keypad. When the selection is completed, depress the ENTR softkey. This causes the VFDT to display a screen similar to screen [2] reflecting the newly updated byte data.

> **Note :**
> The data entered into the 8-bit byte is stored into a battery protected RAM. As a result, the value stored remains even after the instrument is turned off.

When the 440B is equipped with option 03 and a plug is inserted in the 64 kb/s DATA INPUT jack associated with this option, the momentary depression of the DATA key causes the VFDT to display screen [4] below. At the same time, the MESSAGE EXT LED is turned on to remind you that the external data source is used.

Screen [4]



This screen prevails until the plug is withdrawn or another menu is called.

To supply externally the 64 kb/s stream to be carried by the selected DS0 channel, the signal source must be synchronized with the timing signal delivered by the 5 pin connector labeled XMT TIMING SOURCE. The synchronized source output must then be patched to the jack labeled 64 kb/s DATA INPUT. The signal delivered by the external source must have a unipolar format.

Remark:

- When the 8 kHz clock signals delivered by the XMT TIMING SOURCE connector must have the same phase as the 8 kHz clock signals delivered by the RCV TIMING SOURCE connector, the rear panel switch S4 position 10 must be set to ON. When set to OFF, the two clocks have an arbitrary phase relationship.

Additional information regarding the interface requirements for the option 03 are given in chapter 19.

APPLICATION INFORMATION

10.4 The optional data sending capability provided by the 440B can be used most effectively for performing a number of data channel tests. These tests include :

- sending a QRS sequence to perform data transmission evaluation and trouble shooting
- sending stress patterns
- sending test codes as required by DDS maintenance practices
- generating 64 kb/s data pattern
- using the TPI 108/9 RT

In this section some information is given on each of these applications. It should be noted that the proposed tests are not specific to a configuration, in other words, these tests may be carried out while the 440B is used in the stand alone mode or in any drop-and-insert mode. These modes are described in chapters 14 and 15 respectively.

DS0 Channel QRS Simulation

When you need to check the transmission integrity of a 64 kb/s data channel, the most practical way is to send in the desired channel a standard QRS pattern. Either the 511 or the 2047 patterns can be sent into a

channel. When a DS0 QRS pattern receiver monitors the bit stream, it can detect and generally count the number of corrupted bits observed during the test period. From this count, block error counts and bit error rate (BER) can be obtained. If the 440B DS0 DATA receiver is used, all these measurements can be provided. Refer to page 5.2 for more details on this subject.

DS0 Channel Stress Testing

In addition to carrying-out BER type measurements, it is many times helpful to stress the data transmission channel by feeding bit sequences exhibiting extremes in pulse density. This can be readily accomplished by setting the DS0 data generator in the byte mode and selecting the desired mix of 1's and 0's. The 440B DS0 DATA receiver is automatically primed to compare the monitored DS0 sequence with the sequence sent and any difference is identified as a bit error. As a result, you may readily determine if the observed BER is a function of the patten density or any other bit pattern statistics.

DS0 Channel DDS Test Codes

The user-defined byte pattern provided by the bit pattern generator can also be used for generating some of the test patterns commonly used for maintaining the DDS network. For convenience, table 10.1 on the following page identifies 7 such codes.

Code	Description	
X1111110	IDLE CODE	X = solid 1
00101100	DSU LOOPBACK	or solid 0
00101000	CHAN LOOPBACK	
00101010	OCU LOOPBACK	
00011010	MUX OUT OF SYNC	
00011100	TEST CODE	
00011000	UASGN MUX CHAN	

Table 10.1 DDS Test Codes

Remark

To verify that the byte entry has been made correctly, you may patch the DS1 Transmit 1 PCM OUTPUT jack to either DS1 Receiver and display the received data by momentarily depressing twice the DS0 DATA key located below the VFDT. If the pattern is recognized its description appears next to the bit histogram. Screen [5] below illustrate the DS0 DATA display when the MUX OUT OF SYNC code is decoded.

Screen [5]

DSO Bits	:	12345678	#1
MUX OUT OF SYNC		00011010	RCVR NXT

■ ■

Note :
The display does not show the 1-0 sequence, instead it shows a lit rectangle for a 1 and a blank character for a 0.

64 Kb/s Data Pattern Generation

If the 440B is equipped with option 03, it is possible to use the instrument as a 64 kb/s data signal source similar to the KS 20909 data test set.

This is accomplished by accessing the content of the selected DS0 channel in the DS1 stream delivered by the DS1 Transmit 1 section output. To this end, you simply need to patch either the MON or the T1 PCM output from the DS1 Transmit 1 section to either DS1 Receiver PCM input and to display the DS0 DATA content of the selected channel for the DS1 receiver used. The data displayed by the VFDT is simultaneously available at the 64 kb/s DATA output jack on the option 03 panel.

When configured in this manner, any data pattern inserted in the selected DS0 channel in the DS1 Transmit 1 section can be supplied to the outside world at the 64 kb/s rate and used to drive a DS0 data channel unit. The 8 KHz and the 64 KHz clocks associated with the 64 Kb/s data are supplied on the 5 pin connector labeled RCV Timing Source.

Using the TPI 108/9 RT

While the TPI 108/9 RT combines in one set the capabilities of both the TPI 108A and 109A, it has a single access for timing synchronization. When this instrument is to be used jointly with the 440B, it is recommended to set the rear panel switch S4 position 10 to ON. This ensures that both timing sources on the option 03 have identical phases. Consequently, you may connect the TPI timing cable to either 5 pin connector on the 440B when S4/10 is set to ON.

When not using the TPI 108/9 RT, it is recommended that you set this switch in the OFF position.

11. DS0 CHANNEL VF/TONES SIMULATION

INTRODUCTION

11.1 Both of the 440B DS1 Transmit sections are capable of encoding an externally supplied VF tone or signal into a selected DSO channel and to deliver same onto the PCM output. However, because these two sections are not intended to perform identical functions, their capabilities in this regard are not the same. In this chapter you will find:

- a description the tone/VF simulation capability associated with each DS1 Transmit section
- directions for operating the tone/VF sending capability in the DS1 Transmit 1
- directions for operating the tone/VF sending capability in the DS1 Transmit 2
- application information

DSO TONE/VF SIMULATION CAPABILITY DESCRIPTION

11.2 The 440B offers two basic choices when the selected DS0 channel in the DS1 Transmit 1 is to contain an encoded analog signal: a selection of internally generated discrete tones or the encoding of externally supplied VF signals.

The selection of internal tones includes approximately 250,000 level frequency combinations. These tones are generated by a digital signal synthesizer providing highly accurate and stable signals in the frequency range of 50 Hz to 3990 Hz and over the level range of +3.2 dBm0 to -59.9 dBm0. The frequency can be set by steps of 10 Hz nominal and the level by steps of .1 dB. Its should be noted that in reality, to avoid generating tones that are precise sub-harmonics of the 8000 Hz sampling rate, the frequency is always a multiple of 10.036 Hz instead of 10.000 Hz. In practice, this causes the actual frequency delivered by the built-in tone generator to be 1004 Hz when the entered value reads 1000 Hz.

Tones or other VF signals may be supplied externally and are encoded by a Mu-law encoder to yield a 64 kb/s bit stream. This process is completely identical to the VF/digital conversion performed by a conventional DS1 channel bank. To be accepted without introducing any significant amount of distortion, the VF signal must be in the 300 to 3300 Hz frequency range and not exceed +3.2 dBm0.

When the selected DS0 channel in the DS1 Transmit 2 is to contain an encoded VF signal, this signal must be supplied by an external source exclusively. This results from the fact that only the DS1 Transmit 1 is equipped with a digital tone synthesizer. The operation of the DS1 Transmit 2 Mu-law encoder is as described in the preceding paragraph.

The next paragraph provides set-up information.

SETTING-UP THE DS1 TRANSMIT 1 TONE/VF SENDING CAPABILITY

11.3 When the DS1 Transmit 1 section is operated in the stand alone mode, the selected DS0 channel contains a digitally encoded signal whenever the TONE key/LED is either steadily lit or in the FLOSO state. When the DS1 Transmit 1 section is operated in the THRU mode, the DSO channel selection is active only if the SET key/LED is not lit. If lit, the selection can be activated by the momentary depression of the SET key.

When depressing the TONE key, the FLOSO state is transferred to this key and the screen displayed by the VFDT depends on whether a plug is inserted in the EXT VF INPUT jack.

When a plug is not inserted in the EXT VF INPUT jack, the momentary depression of the TONE key causes the VFDT to display a screen similar to screen [1] below. At the same time, the MESSAGE INT LED is lit to indicate that the built-in tone synthesizer is the source of the signal delivered to the selected DS0 channel.

Screen [1]

TONE	dBm0	Hz				ALT
#1	0.0	410	▲	<	>	TONE
			■	■	■	■

In the actual screen, the sign position has a flashing underline. The screen can be edited by moving the underline as required using the arrow softkeys and by

entering the desired numeric values with the keypad for the level and the frequency. Any level value in the range of +3.2 to -59.9 is accepted; likewise, any value for the frequency in the range of 50 Hz to 3990 Hz is accepted. When an attempt is made to enter a value outside of these ranges, the entry is not accepted and the HELP key LED flashes to indicate that the depression of the HELP key will supply the reason for the denial.

When the ▲ softkey is depressed while the ALT key LED is off, the underlined position is incremented by one count. When this softkey is depressed while the ALT key LED is lit, the underlined position is decremented by one count. If the softkey is held depressed, the action is repeated at the rate of four counts per second. This feature provides for stepping quickly up or down by a fixed amount.

Upon depressing the ALT TONE softkey in screen [1], a screen similar to screen [2] is displayed.

Screen [2]

TONE	dBm0	Hz				ALT
#1	0.0	1010	▲	<	>	TONE

Up to 16 tone level/frequency combinations can be stored by the 440B memory. This memory is battery protected and thus its content is not lost when the set is powered down. Successive tones are accessed by depressing momentarily the ALT TONE softkey. If you wish to select the previous tone again, you can speed-up the access by depressing first the ALT key/LED and then the ALT TONE softkey. When it is desired to implement a tone sequence shorter than 16, you may enter an * instead of a digit in any of the parameter position. The * is entered by first momentarily depressing the ALT key and then the * key in the keypad. When this is done, both parameter fields are filled with * and the screen is as illustrated by screen [3] below.

Screen [3]

TONE	dBm0	Hz				ALT
#6	***.*	****	▲	<	>	TONE

When this tone selection prevails, the content of the selected DS0 channel is idle (11111111) and thus the quiet termination is provided.

The momentary depression of the ALT TONE softkey in screen [3] causes the display of the parameters of TONE #1. To extend a tone sequence having fewer than 16 tones, you simply need to replace the two fields containing *'s by a set of legitimate values.

The 16 tone level/frequency combinations originally set at the factory are listed in table 11.1. These combinations are stored in EPROM's and can be downloaded to the battery powered RAM when required. To restore the factory selection, refer to the information given on page 3-2 of this manual.

Tone #	Level (dBm0)	Frequency (Hz)	Prog'd Freq. (Hz)
1	0.0	402	400
2	0.0	1004	1000
3	0.0	2807	2800
4	-10.0	402	400
5	-10.0	1004	1000
6	-10.0	2807	2800
7	-13.0	402	400
8	-13.0	1004	1000
9	-13.0	2807	2800
10	-16.0	402	400
11	-16.0	1004	1000
12	-16.0	2807	2800
13	-20.0	402	400
14	-20.0	1004	1000
15	-20.0	2807	2800
16	-30.0	1004	1000

Table 11.1 Factory Selection For The 16 Tones

When a plug is inserted in the EXT VF INPUT jack, the momentary depression of the TONE key causes the VFDT to display a screen similar to screen [4] below. At the same time, the MESSAGE EXT LED is lit to indicate that an external signal is supplied to the selected DS0 channel.

Screen [4]

The internal TONE is preempted by
the externally supplied VF signal

To be properly encoded, the VF signal applied to the EXT VF INPUT jack should not exceed +3.2 dBm across the 600 Ohm input impedance. When this level is exceeded, the EXT VF OVERLOAD LED is lit and the signal is clipped prior to encoding. The

applied VF signal should be in the 300 to 3300 Hz frequency range.

It should be noted that the selection of the DSO channel content is quite unrelated to the content of the other channels.

SETTING-UP THE DS1 TRANSMIT 2 TONE/VF SENDING CAPABILITY

11.4 When the DS1 Transmit 2 section is operated in the stand alone mode and no patch cord is inserted in the DS1 Transmit 2 VF Input jack, then the selected DS0 channel contains a digitally encoded quiet termination whenever the DS1 #2 selection in channeling either IDLE or 1005 Hz/-20 dBMO. When a patch cord is inserted in the VF input and DS1 #2 selection is IDLE or 1005 Hz/-20dBMO, then the patched-in signal is encoded into the selected channel. When the DS1 Transmit 2 section is iperated in the THRU mode, the selected DS0 channel unconditionally contains the encoded sample values of the signal received at the VF input jack.

The DS0 channel number selection in the DS1 Transmit 2 section is the same as the channel number selected in the DS1 Receiver 2 section. The VF encoder used in this section is identical to the one used in the DS1 Transmit 1 section. Consequently, the same criteria for low-distortion encoding apply.

APPLICATION INFORMATION

11.5 The built-in tone sending capability provided by the 440B can be used most effectively for performing a number of test on the VF receive half-channels. These tests include :

- receive gain alignment
- receive frequency response/gain slope
- receive gain linearity

In this section some information is given on each of these applications. It should be noted that the proposed tests are not specific to a configuration, in other words, these tests may be carried out while the 440B is used in the stand alone mode or in any drop-and-insert mode. These modes are described in chapter 14 and 15 respectively.

Receive Gain Alignment
When a D-bank channel units decodes a calibrated 64 kb/s encoded tone, the channel unit receive gain can be adjusted to let the magnitude of the delivered VF signal match a specified value. In practice, it is common to send a digitally encoded tone of 1004 Hz at 0 dBm0 to the receive half-channel and to measure the VF signal delivered by the receive port while this port is properly terminated.

The 440B can be used to simultaneously deliver the calibrated 64 kb/s tone and to measure the VF signal delivered by the receive half-channel into a 600 ohm termination. The required set-up is illustrated in figure 11.1 on the following page.

To measure the VF tone delivered by the channel unit, the DS1 #2 selection (in DS1 Transmit 2) must be set to 'CHANNELIZED'. It is not important whether the channelized selection is IDLE or 1005 Hz/-20 dBm0. The measurement is obtained by displaying the first screen in the DS0 VF menu. In this screen, the RCX selection must be #2.

Receive Frequency Response/Gain Slope Check
To perform this test, refer to the set-up illustrated in figure 11.1. The frequency response of the receive half channel is obtained by plotting on a graph the level measured by the 440B TMS for each frequency of the DS0 tone sent by the DS1 Transmit 1 section to the channel bank under test. To ensure good accuracy of the results, the tone level must remain unchanged for the duration of the test.

The resolution of the frequency response is increased by reducing the size of the frequency steps. This results in taking more measurements and requires more time. The 440B DS0 tone programming feature can be used to advantage as it allows you to pre-store up to 16 tones and to call them up sequentially. Consequently, to obtain a measurement point, you simply need to enter the following sequence :

- depress the TONE key in the DS1 Transmit 1 section
- depress the ALT TONE softkey to obtain the next tone selection
- depress the DS0 VF key in the Control and Measurements section

Receive Gain Linearity Check
The gain linearity check consists in comparing the set of measurements obtained by measuring the VF level delivered by the decoder under test with the set of 64 kb/s encoded tone signal level values sequentially applied to the channel unit under test.

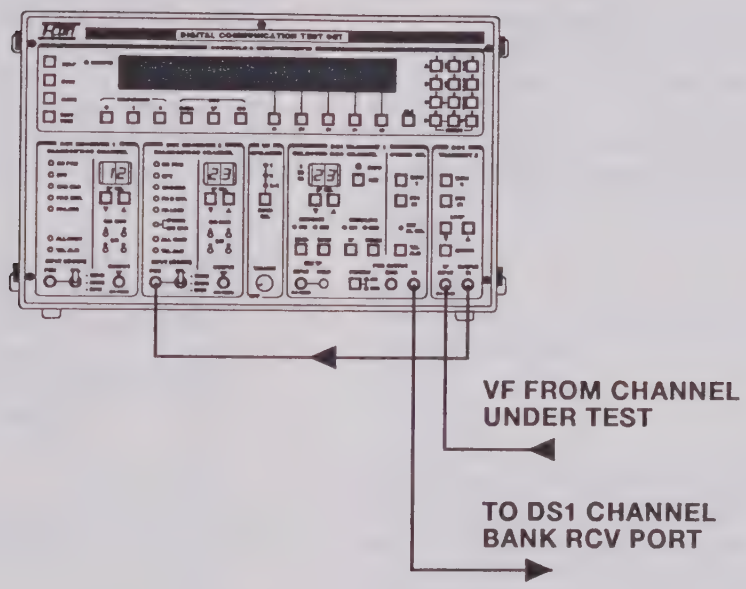


Figure 11-1. Receive Half-Channel Gain Alignment

By plotting the set of input levels on one axis and plotting the set of values read on the 440B on the other axis of a rectangular coordinate system, all deviations from a line inclined by 45° illustrate the gain non-linearity for the receive half-channel. To speed-up the testing, you may want to use the tone pre-storing technique described in the previous paragraph.

Analog Tone Signal Generation

Although the 440B is a digital test set, it can readily be used for generating analog tones as well as digital ones. Analog tones can indeed be obtained by decoding the content of the digital tones inserted into a DS0 channel. To this end, you simply need to patch either the MON or the T1 PCM output from the DS1 Transmit 1 section to either DS1 Receiver PCM input and to obtain the analog tone from the VF output jack in that receiver. This jack supplies the decoded signal in the selected DS0 channel. The source impedance of the analog tone generator is 600 ohm nominal. This source can deliver a useful signal in the range of 3.0 to -50 dBm over the frequency range of 100 Hz to 3500 Hz.

> **Note:**
> When the signal frequency exceeds 3300 Hz, the gain accuracy is reduced.

12. DS0 CHANNEL SUPERVISION SIMULATION

INTRODUCTION

12.1 The signaling content of the selected DS0 channel in the bit streams delivered by the 440B DS1 Transmit 1 and DS1 Transmit 2 sections can be arbitrarily selected by the user. This is of great utility to simulate on-hook, off-hook, or any other supervisory conditions. Because the two DS1 Transmit sections do not have the same functions, their signaling capabilities are not identical. In this chapter you will find :

- a description the signaling simulation capability associated with each DS1 Transmit section
- directions for operating the signaling sending capability in the DS1 Transmit 1
- directions for operating the signaling sending capability in the DS1 Transmit 2
- application information

SIGNALING SIMULATION CAPABILITY DESCRIPTION

12.2 The DS1 Transmit 1 section provides two choices with regard to signaling in the selected DS0 channel. You can either set the state of the A and B bits (A, B, C and D bits when the system format is ESF) manually or by applying externally supplied signaling from a signaling test set for example. The external signaling input requires a single contact closure to ground or an open to signal a 1 or a 0 state respectively. The input can also accept -48 VDC. The signaling states can be combined with the tone/VF signal in the following manner :

- internal tones with internal signaling states
- internal tones with external signaling states
- external VF with internal signaling states
- external tones with external signaling states

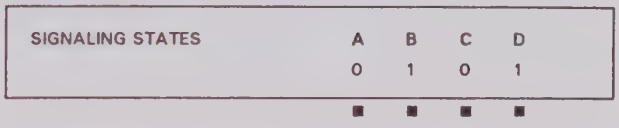
The DS1 Transmit 2 section is more limited, it provides only a manual selection of the signaling bits. Consequently, in the DS0 channel delivered by this section, the manually selected signaling states are always combined with the externally supplied VF signal.

The next paragraph provides set-up information.

SETTING-UP THE DS1 TRANSMIT 1 SIGNALING SENDING CAPABILITY

12.3 The signaling state entry is only meaningful when the content of the selected DS0 channel is TONE or EXT VF. When the TONE key/LED is either solidly lit or is in the FLOSO state, the momentary depression of the STATE key/LED causes the VFDT to display a screen similar to screen [1] if no plugs are inserted into either SIG INPUT jack on the instrument rear panel.

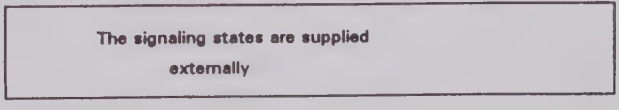
Screen [1]



The absence of plugs in either SIG INPUT jack is indicated by the lit INT SIGNALING LED located above the STATE key. In screen [1] the C and D headings and corresponding digits are blanked out if the system selection is not ESF. The selection can be changed at any time by momentarily depressing the softkeys under the 4 (or two if not ESF) digits on the lower line. Each softkey depression causes the displayed value to toggle between 1 and 0. The signaling states in the selected channel are continually updated to reflect the currently displayed states. Following power up, every signaling bit is automatically set to state 1.

Whenever a plug is inserted into either SIG INPUT jack, the INT SIGNALING LED turns off and the EXT SIGNALING LED turns on. At the same time the VFDT displays the screen [2] below when the STATE key/LED is in the FLOSO state.

Screen [2]



If the plugs are withdrawn from SIG INPUT jacks, the EXT SIGNALING LED turns off and the INT SIGNALING LED turns on.

When a plug is inserted in either SIG INPUT jack, the signaling content of the selected DS0 channel is

automatically controlled by the applied signal if any. The bit assignment for each input jack is silkscreened on the panel and is reproduced in table 12.1 along with the assigned states.

Jack	Bit	State	Circuit
J17 Tip to sleeve	A	0	> 4 V or open
J17 Ring to sleeve	B	1	< 1 V or closure
J18 Tip to sleeve	C		
J18 Ring to sleeve	D		

Table 12.1 External signaling inputs

Appropriate circuit protection is provided against applied voltages in excess of 50 volts with respect to ground.

SETTING-UP THE DS1 TRANSMIT 2 SIGNALING SENDING CAPABILITY

12.4 The signaling states for the DS0 channel selected by the DS1 Receiver 2 section are set by the switch S3 on the rear panel. The switch has four on/off positions to control respectively the state of the signaling bit A, B, C and D. When a switch is set to OFF, the corresponding bit takes the value 0. Conversely when setting the switch to ON the corresponding bit takes the value 1.

The switch is always active when the DS1 Transmit 2 delivers a channelized bit stream.

APPLICATION INFORMATION

12.5 The ability to arbitrarily set the state of the signaling bits in a selected DS0 channel makes it possible to verify that the receiving channel unit does indeed recognize and asserts the on-hook and off-hook states and ignores incompatible signaling state entries. Additionally, the external signaling input jacks associated with the DS1 Transmit 1 section allow you to use a signaling test set to simulate the sending of a DP encoded telephone number and to measure the pulse distortion introduced by the receiving channel unit. In this case, a second signaling test set must monitor the receive signaling lead(s).

Additional information is provided in the next chapter with regard to testing for pulse distortion.

13. DS0 CHANNEL TELEPHONE No. SIMULATION

INTRODUCTION

13.1 When equipped with option 06, the 440B DS1 Transmit 1 DS0 section is capable of sending a sequence of digits and other symbols required to simulate the transmission of MF, DTMF and DP encoded telephone numbers. This capability has a number of practical applications, of which the operational check of telephone number decoders is but the most obvious. In this chapter you will find:

- a description the MF, DTMF and DP encoded telephone number simulation capability
- directions for editing and sending MF encoded telephone No's
- directions for editing and sending DTMF encoded phone No's
- directions for editing and sending MF encoded telephone No's
- application information

If the 440B is not equipped with option 06, the content of this chapter is not directly applicable to the operation of the instrument.

MF, DTMF and DP TELEPHONE NUMBER SIMULATION CAPABILITY DESCRIPTION

13.2 A battery powered memory in the 440B contains up to 16 telephone numbers. Each number consists of up to 35 digits or other symbols such as pauses, on-hook, off-hook etc... These numbers can be stored and edited by the user as required using a sequence of EDIT screens and commands. The set of factory selected numbers, listed in table 13.1, can always be restored in the memory and replace the user-entered numbers. (The procedure for doing this is described on page 3.2)

The factory selections for MF and DTMF digit duration and interdigit duration are set at 50 ms each. The factory selection for DP parameters are set as follows: 10 PPS, 61 % break and 500 ms interdigit time.

As a rule, MF and DTMF encoded numbers occupy 7 and 5/6 bits per sample in the selected DS0 channel while the supervision occupies the 1/6 bits. DP encoded numbers occupy only 1/6 bits per sample; in this case, the other 7 and 5/6 bits are set to 1.

Each telephone number in the memory bank can be selected and displayed on the VFDT and, when needed, sent at a specified rate. As previously noted, you can edit these numbers quite liberally when required. For example, MF and DTMF numbers can be specified for digit duration, interdigit interval and tone level. For DP encoded numbers, you can specify the digit sending rate, the percent break and the interdigit pause. In all three encoding schemes, the on-hook and off-hook states can be individually encoded with the A, B, C and D signaling bits.

For added flexibility, the telephone numbers can be conditionally sent upon receipt of a wink by DS1 Receiver 2. Likewise, DTMF encoded numbers can simulate a foreign exchange loop start configuration (FX/LS), a foreign exchange ground start configuration (FX/GS) or the E & M configuration.

The next section provides general set-up information for letting the DS1 Transmit 1 section send encoded telephone numbers.

GENERAL INFORMATION FOR SENDING AN ENCODED TELEPHONE NUMBER.

13.3 Independently of the chosen encoding method, to send a encoded telephone number in the DS1 Transmit 1 DS0 selected channel, you need to carry out the following steps :

1. enable the channel number selection if the THRU mode prevails by depressing the SET key
2. depress the No. key to display the current telephone number selection
3. if desired, select another number by depressing the NXT softkey (or the ALT/NXT key combination)
4. edit the number as required
5. send the number by depressing the GO softkey.

The momentary depression of the No. key causes the transfer of the FLOSO state to this key/LED and the display of screen [1] if the option 06 is not installed in the 440B.

Screen [1]

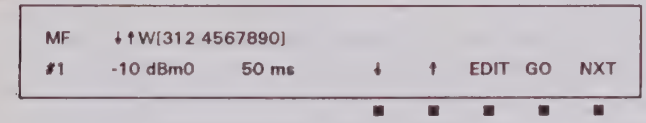
The Telephone No. option 06 must be installed to activate this feature.

#		Telephone No.	Type	On-H ABCD	Off-H ABCD	R to S ABCD
1	↓↑	[123♦56789012345]	MF	0000	1111	n/a
2	↓↑	*123♦4567890ABCD#	DTMF-E&M	0000	1111	n/a
3	↓↕	*123♦4567890ABCD#	DTMF-FX/GS	0101	1111	0000
4	↓↑	*123♦4567890ABCD#	DTMF-FX/LS	0101	1111	n/a
5	↓↑	123♦4567890123456	DP	0000	1111	n/a
6	↓↑	W[123♦4567890123]	MF	0000	1111	n/a
7	↓↑	W123♦456789012345	DP	0000	1111	n/a
8	↓↑	[112♦23344556677]	MF	0000	1111	n/a
9	↓↑	[889♦90011223344]	MF	0000	1111	n/a
10	↓↑	112♦2334455667788	DTMF-E&M	0000	1111	n/a
11	↓↑	990♦0AABBCCDD**##	DTMF-E&M	0000	1111	n/a
12	↓↑	112♦2334455667788	DP	0000	1111	n/a
13	↓↑	990♦0112233445566	DP	0000	1111	n/a
14	↓↑	[10♦101010101010]	MF	0000	1111	n/a
15	↓↑	*10♦101010101010#	DTMF-E&M	0000	1111	n/a
16	↓↑	101♦1010101010101	DP	0000	1111	n/a

Table 13.1 Factory selected telephone numbers

If option 06 is installed, a screen similar to screen [2] appears instead.

Screen [2]



This screen offers you a number of choices. By depressing the on-hook softkey (↓), the on-hook signaling status is sent. Alternatively, by depressing the off-hook softkey (↑), the off-hook status is sent. Upon depressing the GO softkey in screen [2], the sending of the telephone No. displayed on the first line of the screen is initiated.

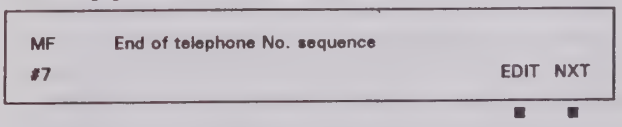
When in screen [2] the NXT softkey is depressed, the next telephone No. in the sequence (#3 in this example) is displayed. When the ALT key is depressed prior to the NXT key in screen [2], the next screen displayed has # n-1.

The content of the screen [2] can be changed by the user by depressing the EDIT softkey. The editing feature allows a user to fully define both the phone number to be sent and the signaling (supervision) in the channel. Encoding of telephone No's can be made with DTMF and DP in addition to MF. It is also possible for a user to select a limited sequence of telephone No's for example the sequence of the first 6 No. selections. To do this, the user must depress the EDIT softkey when the #7 telephone No. is displayed. When this is done, screen [3] is displayed.

Screen [3]

With the pointers, the underline [not shown] can be placed under any one of the three encoding selections or the LAST# heading. When in screen [3] the LAST# heading is underlined, the depression of the NXT softkey yields the screen [4].

Screen [4]



When the EDIT softkey is depressed in screen [4], the edit screen [3] is displayed anew. If the NXT softkey in screen [4] is depressed the telephone #1 is displayed.

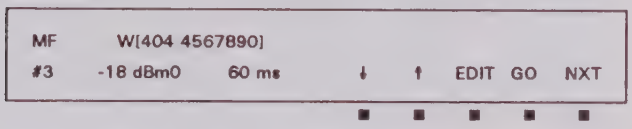
The following three sections provide an extensive discussion of each of these three encoding methods.

MF ENCODED TELEPHONE No's.

13.4 This section covers the editing of MF encoded phone No's and describes the sending process of an MF encoded No.

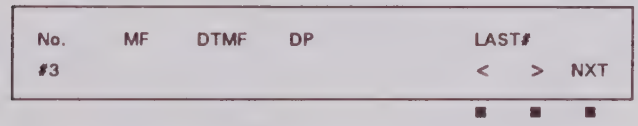
Editing.
When the VFDT displays a telephone No. as for example screen [3] below, this number can be changed as required by following the sequence of screens [4] through [8].

Screen [3]



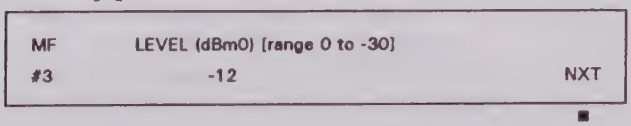
When in screen [3] the EDIT softkey is depressed, screen [4] is displayed.

Screen [4]



With the pointers, the underline [not shown] can be placed under any one of the three encoding selections or the LAST# heading. If the NXT softkey in screen [4] is depressed when the MF heading is underlined, screen [5] is displayed.

Screen [5]



When screen [5] is displayed, the level data field can be set to any value in the specified range. Any attempt to enter an out-of-range value is rejected and results in causing the HELP key LED to flash. The depression of the HELP key yields the reason for the denial. Depressing the NXT softkey in screen [5] when the data is in the acceptable range causes the display of screen [6].

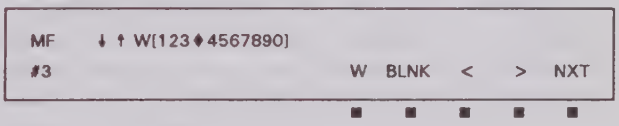
Screen [6]

The operation of the softkey in this screen is consistent with the operation described in previous screens. The underline [not shown] assists the user in the editing. The specified duration range applies to both the symbol and the intersymbol duration. Depressing the NXT softkey in screen [6] causes the exit from this screen and the display of screen [7].

Screen [7]

The default values for the on-hook (↓) and off-hook (↑) signaling states are given in screen [7]. They can be changed by using the pointer softkeys and the 1 and 0 keys exclusively. ABCD states are shown whether the ESF format is selected or not. Upon depressing the NXT softkey in screen [7] screen [8] is displayed.

Screen [8]



When the W softkey is depressed, the W (wait for wink) character is displayed in the number as shown in screen [8]. It is possible for a telephone number to have several winks. (An example of this may be the feature group D.)

Upon initial display of screen [8], the underline (not shown) is blinking under the leftmost data field in the first row(↓). With the help of the pointer softkeys the underline can be placed anywhere in the 35 symbol field provided that a non-blank symbol precedes the character position or that it is the left-most location in the field. The acceptable symbols include only those entered via the numeric keys 0-9, the keys labeled KP, ST, STP, ST2P, ST3P, P/♦, +/↑, -/↓ and the softkeys W and BLNK. The attempted entry of any other symbols is rejected. The symbols displayed for the non-numeric key entries are as listed in Table 13.2.

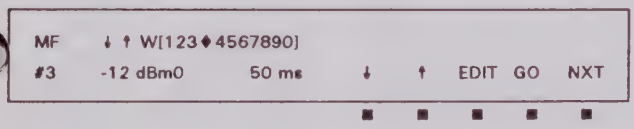
Keys	Display	Keys	Display
KP	[	P/♦	♦
ST	]	+/↑	↑
STP	-	-/↓	↓
ST2P	=	W	W
ST3P	≡	BLANK	

Table 13.2 Special MF symbols

When the BLANK softkey is depressed, the underlined location and all the locations on the right of the underline are cleared. When the W softkey is depressed, the W character is entered at the underlined location. Normally, MF encoded telephone numbers start with KP ([) and end with ST (]). The total number of symbols available for any telephone number cannot exceed 35.

The depression of the NXT key in screen [8] causes the exit and the display of the newly edited screen. An example of this screen is given by screen [9].

Screen [9]



In screen [9]
- the ↓ represents the on-hook condition
- the ↑ represents the off-hook condition
- the W is a 'wait for wink' symbol
- the [represents the KP (key pulse)
- the ♦ represents a 2 second pause
- the] represents the ST (stop pulsing)
- the actual number is 123 4567890
- the RMS level of each tone is -12 dBm0
- the duration of an MF encoded symbol is 50 ms
- the telephone number is the third one in the sequence of up to 16 different numbers

Remarks :
- The ON-HOOK symbol (↓) must generally be used to initialize the state of the signaling in the channel. This symbol, when executed, causes the signaling bits in this channel to reflect the on-hook state for a nominal duration of one second.

- The OFF-HOOK symbol (↑) must generally precede any other symbol except for the on-hook symbol. The execution of the off-hook symbol causes the signaling bits in this channel to reflect the off-hook state.

Sending process.
When in screen [9] the GO softkey is depressed, the sending of the displayed phone number, along with all the supervision symbols and corresponding states, is initiated.

While the string of symbols is being dispatched, the GO heading flashes on and off at the rate of 2 flashes per second. When the string has been fully executed, the flashing stops. While a wink is awaited, the corresponding W in the telephone No. string is underlined. If for any reason, the expected wink has not been received and the sending process is held-up, the GO state can be exited by entering ALT and then the GO. As this sequence is terminated, the underline, if any is turned off and the number sequence can be sent over again. The sending of a telephone No. sequence can also be aborted by depressing either the TONE or the DATA keys.

While the GO key is flashing, all the other softkeys are disabled. When the on-hook (↓) symbol is executed as part of a symbol string, its execution takes 2 seconds. When the off-hook (↑) symbol is executed as part of a symbol string, the next symbol execution is delayed by 100 milliseconds.

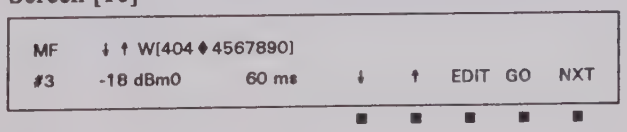
When the DS0 channel is not carrying a tone encoded character, each byte in the selected channel is 1111111x. The least significant bit x has value 1 in every frame except possibly during signaling frames where the value is set by the signaling state.

DTMF ENCODED TELEPHONE No's.

13.5 This section covers the editing of DTMF encoded phone No's and describes the sending process of a DTMF encoded No.

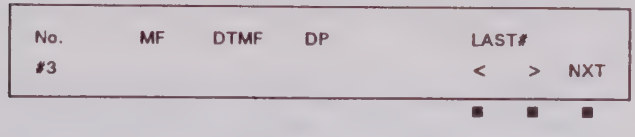
Editing.
When the VFDT displays a telephone No. as for example screen [10] below, this number can be changed as required by following the sequence of screens [11] through [18].

Screen [10]



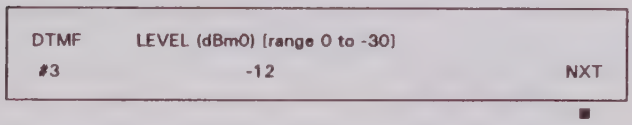
When in screen [11] the EDIT softkey is depressed, screen [12] is displayed.

Screen [11]



With the pointers, the underline [not shown] can be placed under any one of the three encoding selections or the LAST# heading. If the NXT softkey in screen [11] is depressed when the DTMF heading is underlined, screen [12] is displayed.

Screen [12]

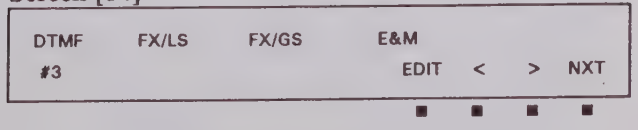


When screen [12] is displayed, the level data field can be set to any value in the specified range. Any attempt to enter an out-of-range value is rejected and results in causing the HELP key LED to flash. The depression of the HELP key yields the reason for the denial. Depressing the NXT softkey in screen [12] when the data is in the acceptable range causes the display of screen [13].

Screen [13]

The operation of the softkey in this screen is consistent with the operation described in previous screens. The underline [not shown] assists the user in the editing. The specified duration range applies to both the symbol and the intersymbol duration. Depressing the NXT softkey in screen [13] causes the exit from this screen and the display of screen [14].

Screen [14]



With the pointers, the underline [not shown] can be placed under any one of the three signaling headings. If the EDIT softkey in screen [14] is depressed when the FX/LS heading is underlined, screen [15] is displayed.

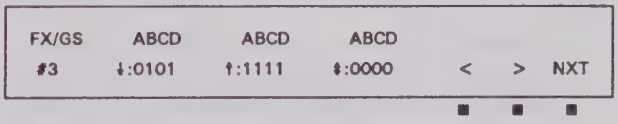
Screen [15]

The default values for the on-hook (↓) and off-hook (↑) signaling states are given in screen [15]. They can be changed by using the pointer softkeys and the 1 and 0 keys exclusively. ABCD states are shown whether the ESF format is selected or not. Upon depressing the NXT softkey in screen [15] screen [16] is displayed.

Screen [16]

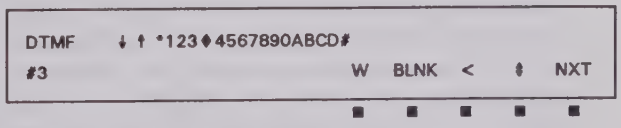
If the EDIT softkey in screen [14] is depressed when the FX/GS heading is underlined, screen [17] is displayed.

Screen[17]



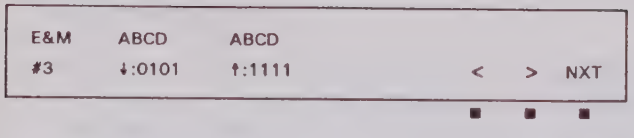
The default values for the on-hook (↓), off-hook (↑) and request-to-send (↕) signaling states are given in screen [17]. They can be changed by using the pointer softkeys and the 1 and 0 keys exclusively. ABCD states are shown whether the ESF format is selected or not. Upon depressing the NXT softkey in screen [17] screen [18] is displayed.

Screen [18]



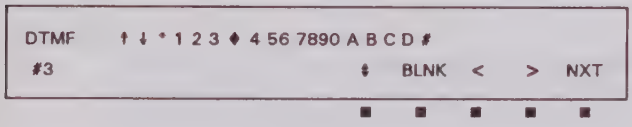
If the EDIT softkey in screen [14] is depressed when the E&M heading is underlined, screen [19] is displayed.

Screen [19]



The default values for the on-hook (↓) and off-hook (↑) signaling states are given in screen [19]. They can be changed by using the pointer softkeys and the 1 and 0 keys exclusively. ABCD states are shown whether the ESF format is selected or not. Upon depressing the NXT softkey in screen [19] screen [20] is displayed.

Screen [20]



Upon initial display of screens [16], [18] or [20] the underline (not shown) is blinking under the leftmost data field in the first row (↓). With the help of the pointer softkeys the underline can be placed anywhere in the 35 symbol field provided that a non-blank symbol precedes the character position or that it is the left-most location in the field. The acceptable symbols include only those entered via the numeric keys 0-9, the keys labeled A, B, C, D, *, #, P/♦, +/↑, -/↓ and the softkeys ↕, BLNK and W. The attempted entry of any other symbols is rejected. The symbols displayed for the non-numeric key entries are listed in table 13.3.

Keys	Display
*	*
#	#
P/♦	♦
+/↑	↑
-/↓	↓
BLANK	

Table 13.3 Special DTMF symbols

When the BLANK softkey is depressed, the underlined location and all the locations on the right of the underline are cleared. When the softkey is depressed, the character is entered at the underlined location. Occasionally, DTMF encoded telephone numbers start with an * and end with a #. The total number of symbols available for any telephone number cannot exceed 35.

The depression of the NXT key in screens [16], [18] or [20] causes the exit and the display of the newly edited screen. An example of this screen is given by screen [21].

Screen [21]

In screen [21]
- the ↓ represents the on-hook condition
- the ↕ represents the request-to-send status
- the * represents the start character
- the ♦ represents a 2 second pause
- the # represents the end of No. character
- the actual number is 123 4567890ABCD
- the RMS level of each tone is -12 dBm0
- the telephone number is the third one in the sequence of up to 16 different numbers

Remarks :
- The ON-HOOK symbol (↓) must generally be used to initialize the state of the signaling in the channel. This symbol, when executed, causes the signaling bits in this channel to reflect the on-hook state for a nominal duration of one second.

- The OFF-HOOK symbol (↑) must generally precede any other symbol except for the on-hook symbol. The execution of the off-hook symbol causes the signaling bits in this channel to reflect the off-hook state.

Sending process.
When in screen [21] the GO softkey is depressed, the sending of the displayed phone number, along with all the supervision symbols is initiated.

While the string of symbols is being dispatched, the GO heading flashes on and off at the rate of 2 flashes per second. When the string has been fully executed, the flashing stops. While an OK to send a telephone No is awaited, the corresponding (request to send symbol) in the telephone No. string is underlined. If for any reason, the expected OK has not been received and the sending process is held-up, the GO state can be exited by entering ALT and then the GO. As this sequence is terminated, the underline, if any is turned off and the number sequence can be sent over again. The sending of a telephone No. sequence

can also be aborted by depressing either the TONE or the DATA keys.

While the GO key is flashing, all the other softkeys are disabled. When the on-hook (↓) symbol is executed as part of a symbol string, its execution takes 2 seconds. When the off-hook (↑) symbol is executed as part of a symbol string, the next symbol execution is delayed by 100 milliseconds.

When the DS0 channel is not carrying a tone encoded character, each byte in the selected channel is 1111111x. The least significant bit x has value 1 in every frame except possibly during signaling frames where the value is set by the signaling state.

Remark

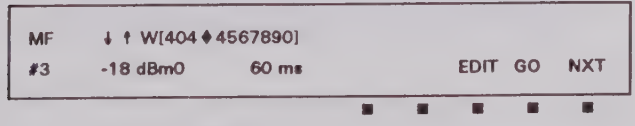
- When the FX/GS supervision is used, the OK to send the telephone number must be received by the RCVR #2 before the tel No. is dispatched. Upon receiving the 'OK to send' signaling state, the 440B sends the off-hook state. The 'OK to send' status is communicated by the far end office by setting the A bit to 0. This bit has normally the state 1.

DP ENCODED TELEPHONE No's.

13.6 This section covers the editing of DP encoded phone No's and describes the sending process of an DP encoded No.

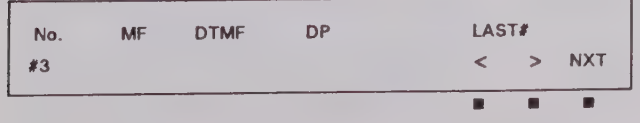
Editing.
When the VFDT displays a telephone No. as for example screen [22] below, this number can be changed as required by following the sequence of screens [23] through [29].

Screen [22]



When in screen [22] the EDIT softkey is depressed, screen [23] is displayed.

Screen [23]



With the pointers, the underline [not shown] can be placed under any one of the three encoding selections or the LAST# heading. If the NXT softkey in screen [23] is depressed when the DP heading is underlined, screen [24] is displayed.

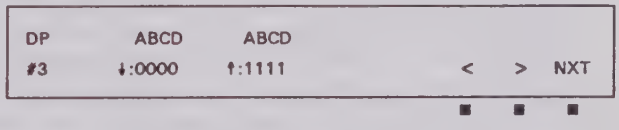
Screen [24]

The editing of screen [24] is consistent with the other screens previously described. The legitimate exit of this screen is obtained by depressing the NXT softkey. This exit yields screen [25].

Screen [25]

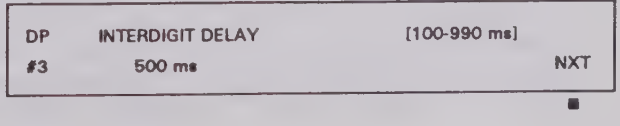
The editing of this screen is self-explanatory. Upon exit, by depressing the NXT softkey, screen [26] is displayed.

Screen [26]



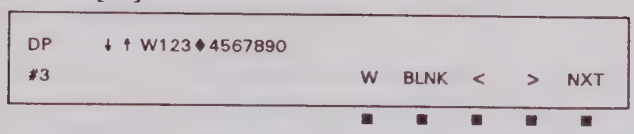
The default values for the on-hook (↓) and off-hook (↑) signaling states are given in screen [26]. They can be changed by using the pointer softkeys and the 1 and 0 keys exclusively. ABCD states are shown whether the ESF format is selected or not. Upon depressing the NXT softkey in screen [26] screen [27] is displayed.

Screen [27]



Screen [27] is edited by entering from the key pad the digits making up the required delay in the specified range. Exit from this screen is obtained by depressing the NXT key and yields screen [28].

Screen [28]



Upon initial display of this screen, the underline (not shown) is blinking under the leftmost data field in the first row (↓). With the help of the arrow softkeys the underline can be placed anywhere in the 35 symbol field provided that a non-blank symbol precedes the underlined location or that it is the leftmost location in the field. The acceptable keys include only the numeric 0-9, P/♦, +/↓, -/↑ and the softkeys W and BLNK. The attempted entry of any other symbols is rejected. The symbols displayed for the non-numeric key entries are as listed in table 13.4.

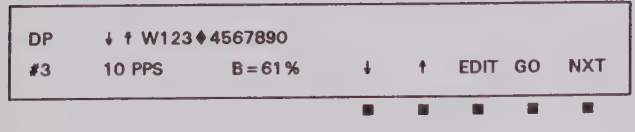
Keys	Display
P/♦	♦
+/↑	↑
-/↓	↓
W	W
BLANK	

Table 13.4 Special DP symbols

When the BLNK softkey is depressed, the underlined location and all the locations on the right of the underline are cleared. When the softkey is depressed, the character is entered at the underlined location. The total number of symbols available for any telephone number cannot exceed 35. When the underline is located at the 35th location and a legitimate symbol is entered, the underline moves back to the first location.

The depression of the NXT key in screen [28] causes the exit and the display of the newly edited screen. An example of this screen is given by screen [29].

Screen [29]



In screen [29]
- the ↓ represents the on-hook condition
- the ↑ represents the off-hook condition
- the W is the 'wait for wink' symbol
- the ♦ represents a 2 second pause
- the actual number is 123 4567890
- the repetition rate is 10 pulses per second (PPS)
- the brake duration is 61% of the pulse period
- the telephone number is the third one in the sequence of up to 16 different numbers

Remarks :
- The ON-HOOK symbol (↓) must generally be used to initialize the state of the signaling in the channel. This symbol, when executed, causes the signaling bits in this channel to reflect the on-hook state for a nominal duration of one second.

- The OFF-HOOK symbol (↑) must generally precede any other symbol except for the on-hook symbol. The execution of the off-hook symbol causes the signaling bits in this channel to reflect the off-hook state.

Sending process.
When in screen [29] the GO softkey is depressed, the sending of the displayed phone No., along with all the supervision symbols is initiated. While the number is being dispatched, the signaling bits in the selected channel take on the specified on-hook and off-hook states and the other bits are set to 1.

While the string of symbols is being executed, the GO heading flashes on and off at the rate of 2 flashes per second. When the string has been fully executed, the flashing stops. While a wink is awaited, the corresponding W in the telephone number string is underlined. If for any reason, the expected wink is not received, the sending process is held-up. The GO state can be exited by entering ALT and then the GO. As this sequence is terminated, the underline, if any is turned off and the number sequence can be sent over again. The sending of a telephone No. sequence can also be aborted by depressing either the TONE or the DATA keys.

While the GO key is flashing, all the other softkeys are disabled. When the on-hook (↓) symbol is executed as part of a symbol string, its execution takes 2 seconds. When the off-hook (↑) symbol is executed as part of a symbol string, the next symbol execution is delayed by 100 milliseconds.

Remark
- In the DP screens no difference is made between delayed dial and wink start. In either case, outpulsing starts nominally 100 ms after the trailing edge of the wink/delay pulse is received.

Application Information

13.7 The 440B can readily be used for delivering all the MF and DTMF encoded telephone numbers described in the preceding sections, as analog signals. This is accomplished by decoding the digitally encoded signals inserted into the selected DS0 channel.

To this end, you simply need to patch either the MON or the T1 PCM output from the DS1 Transmit 1 section to either DS1 Receiver PCM input and to obtain the analog tone from the VF output jack in that receiver. This jack supplies the decoded signal in the selected DS0 channel. The source impedance of the analog tone generator is 600 ohm nominal. This source output level is normalized such that 0 dBm0 = 0 dBm in 600 Ohms.

This analog output can be patched directly to a channel unit under test or a MF/DTMF digit decoder.

14. DS1 TERMINAL MODE EMULATION

INTRODUCTION

14.1 The combination of a DS1 transmitter and a DS1 receiver provided by the 440B can be used to emulate a DS1 channel bank. This emulation can be most useful for testing or characterizing a channel bank prior to its placement in service. The purpose of this chapter is to facilitate the use of the 440B for this application. In this chapter you will find :

- a summary of the tests and measurements performed by the 440B while in the terminal emulation mode
- a description of the most common test set-ups

440B TERMINAL EMULATION MODE TEST CAPABILITIES

14.2 The operation of a typical D-bank can be checked in an out-of-service basis by testing separately the transmit half and the receive half. These may be tested by patching the 440B in the general test configuration shown figure 14.1.

As can be observed from figure 14.1, the digital access to the channel bank under test can be readily obtained at the DSX bay without disconnecting any circuits. Most tests can be carried out with just one DS1 Receiver and one DS1 Transmitter section. The DS1 Receiver provides for the analysis of the DS1 bit stream delivered by the channel bank as well as the decoding of a selected DS0 channel and the measurement of the channel content. Conversely, the DS1 Transmit section simulates the transmit and encoding circuits of the channel bank under test.

When testing the transmit half of the channel bank, the 440B can evaluate the encoding integrity of each DS0 transmit half-channel whether they carry VF, signaling or data. In addition the DS1 Receiver in the 440B can measure the bit rate and the pulse amplitude of the signal delivered by the channel bank as well as verify that the channel bank operates properly in the loop timed mode.

When testing the receive half of the channel bank, the 440B can similarly evaluate the decoding accuracy of each DS0 receive half-channel regardless of their type.

Specific DS0 half-channel transmission measurements you can perform with the 440B include :

- VF level, frequency and noise
- Out-of-band signaling and supervision integrity
- Data encoding & decoding integrity at 64 kb/s and 56 kb/s

Additional tests that may carried-out while the 440B is set-up as in figure 14.1 include :

- loop timing option check
- diagnostics validation

Set-up information for making the above listed measurements is given in the next section.

TEST SET-UP DESCRIPTION

14.3 While the set-ups may differ, the test procedures applicable to the measurements listed above are nearly identical to those given in preceding chapters. To avoid duplication, wherever possible, references are made to those chapters.

To perform DS0 half-channel transmission tests, the 440B system selection must be set to conform to the type of bank under test. The system selection is obtained as described in section 3.4. In addition care must be taken to set the DS1 transmit format to either AMI or B8ZS as required by the bank under test. Failure to do this can result in unreliable measurements. In every cases, the DS1 RCVR input selection must be set to TERM when the PCM input is patched to an out jack.

DS0 VOICE FREQUENCY CHANNEL CHARACTERIZATION

14.3.1 Testing of the transmit half-channel VF parameters is performed as described in section 6.6. When a precise VF signal source is not available for driving the channel under test, you may configure the 440B to supply the desired VF signals as described at the end of section 11.5.

Testing of the receive half-channel VF parameters is performed as described in section 11.5.

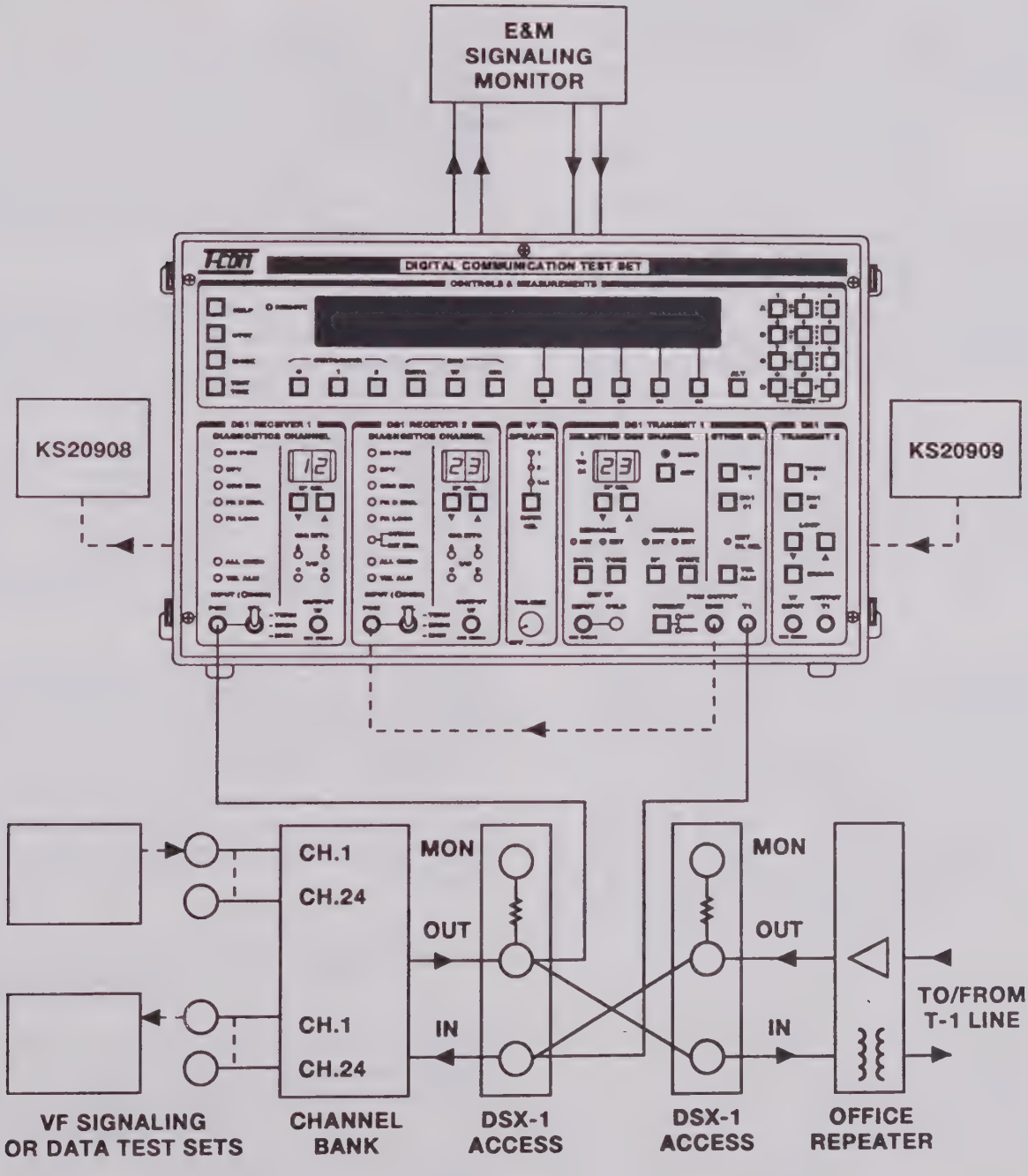


Figure 14-1. Channel Bank Test Configuration

DS0 SIGNALING AND SUPERVISION OPERATIONAL CHECK

14.3.2 The DS0 supervision monitoring capability, described in section 7.2, is most effective to validate the DS0 transmit half-channel signaling and supervision integrity. It allows you to verify that the signaling states in the selected channel are accurately tracking the supervision applied to the channel under test while, at the same time, the other 23 channels are unaffected.

To test the timing integrity of a DS0 transmit half-channel, it is recommended to supply a DP encoded telephone number to this channel and to set-up the 440B to capture the number and to measure the PPS and the % break as described in section 8.3 and 8.4.

To validate the DS0 receive half-channel for supervision integrity, the 440B can be set-up to supply any desired combinations of signaling states (A, B, C, D) as described in section 12.3. This test can be complemented by the sending of DP encoded telephone numbers in the channel under test as described in section 13.6.

It should be noted that the 440B can also be used for evaluating the signaling parameters directly from the signaling circuit. In this case, the signaling terminals are patched to the Transmit 1 EXT SIG input jacks on the rear panel of the instrument while the DS1 Receiver 2 monitors the bits stream delivered by the T1 output from the Transmit 1. The Transmit 1 yields a highly accurate conversion from the signaling to the PCM domain.

DS0 DATA ENCODING & DECODING INTEGRITY CHECK

14.3.3 The DS0 data monitoring/measurement capability, described in section 5 should be used to validate the DS0 transmit half-channel data encoding integrity at 64 kb/s.

To characterize the decoding integrity of a DS0 data channel unit using the 440B, refer to section 10.3.

LOOP TIMING CHECK

14.3.4 To compare transmit and receive clock rates, the patch cord shown in dotted line in figure 14.1. must be in place. Clock synchronization prevails when no slippage is observed on the screen in the STAT/RCVR menu (1 or 2). The occurrence of slippage and the display of slip counts indicate that the channel bank is either not properly optioned or is not operating properly.

DIAGNOSTICS VALIDATION

14.3.5 By letting the 440B simulate various transmission impairments and alarm conditions, the channel bank built-in diagnostics functionality can be verified. The 440B DS1 1 and 2 may be used in combination to deliver bipolar violations, frame bit errors, CRC errors (ESF format only), AIS (all-ones/blue signal) and the remote alarm condition.

To deliver bipolar violations, frame bit errors or CRC errors, the channel bank IN jack must be patched to the 440B DS1 Transmit 2 T1 output. The desired impairment must be selected from the error menu obtained by depressing the ERROR key in the DS1 Transmit 2 section. Refer to section 16.4.1 for additional information.

To deliver the AIS pattern, the channel bank IN jack must be patched to the 440B DS1 Transmit 2 T1 output. The AIS code is obtained by selecting the ALL ONES UFR (unframed) pattern in the DS1 #2 menu. To send remote alarm code the channel bank in jack must be patched to the DS1 Transmit 1 PCM OUTPUT T1 jack. The remote alarm code is sent whenever the LED in the YEL ALM key is lit. This LED is turned on and off alternatively by successive depression of the YEL ALM key.

15. DS1 DROP-AND-INSERT MODES

INTRODUCTION

15.1 When performed by a well trained person, drop-and-insert can provide a number of benefits. The 440B can be configured to provide several useful variations on the basic drop-and-insert test method. It is the purpose of this chapter to acquaint the user with the full range of drop-and-insert tests to which the 440B lends itself. In this chapter you will find :

- an overview of drop-and-insert test applications
- a review and test set-up description of half-duplex and full-duplex drop-and-insert test configurations
- application information on half-duplex drop-and-insert configurations.

WHEN TO CONSIDER DROP-AND-INSERT TESTING

15.2 Drop-and-insert testing is recommended when you need to :

1. identify whether a DS0 channel RCV side or XMT side is defective without turning down the service on the T1 line
2. loop a single DS0 channel back to the sender
3. copy the content of one channel onto another to obtain double feed for comparison testing
4. test echo cancellers
5. dial and talk on a selected DS0 channel

These applications are described in section 15.5. From a practical point of view, drop-and-insert testing only makes sense if you need to access (drop) and insert in a T1 bit stream the content of a specific DS0 channel. Whether the content of this channel is VF (voice), data, signaling or supervision is inconsequential.

NOTE
While the drop-and-insert test techniques described in this chapter can be very useful, their misuse can readily result in loss of traffic. Whenever planning to perform drop-and-insert testing, we strongly recommend to be unhurried and to proceed methodically in following the instructions given herein.

HALF-DUPLEX DROP-AND-INSERT TEST CONFIGURATIONS

15.3 Although the half-duplex drop-and-insert testing configuration has a number of applications, perhaps the most common is to identify the location of a PCM transmission fault without requiring a helper at the remote site.

The 440B may be configured to the half-duplex drop-and-insert test mode in two different ways. The first and most common way is to combine the DS1 Receiver 1 with the DS1 Transmit 1. The second way is to combine the DS1 Receiver 2 with the DS1 Transmit 2. In both cases, the THRU mode prevails.

Figure 1 illustrates the first half-duplex drop-and-insert test mode. When this configuration is established, the DS1 transmission from the far end office to the local channel bank is provided for 23 DS0 channels (out of 24). The content of the channel number selected in the DS1 Receiver 1 section can be analyzed either by the 440B itself or by auxiliary test equipment patched to the receiver VF and signaling output ports. The content of the channel selected by the DS1 Transmit 1 section can be supplied by the 440B itself or from external sources for VF, data, supervision and signaling.

The content of the DS0 channel selected by the DS1 Transmit 1 is normally decoded by the channel bank (or any other terminal equipment) and the signal can be analyzed by various pieces of test equipment. For instance, if the signal introduced by the 440B in DS0 channel #3 is a single tone of 440 Hz at -6 dBm0, a VF level meter patched at the RCV jack #3 should verify that this signal has the correct level. It is thus possible to verify that the bank RCV circuit is operating properly without having to send the test signal from the far-end office.

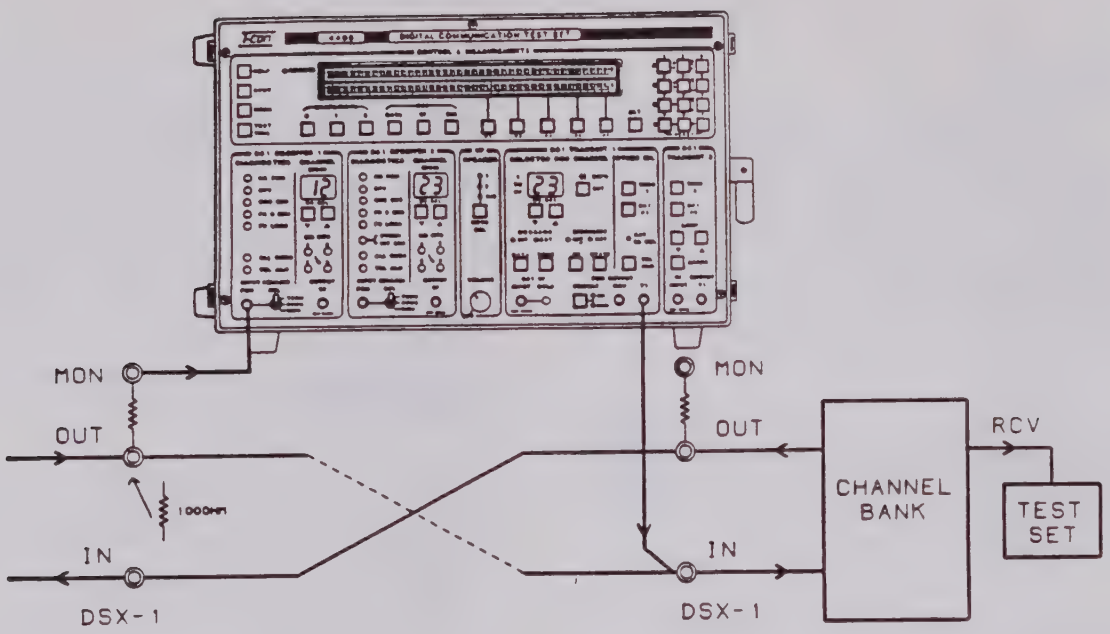


Fig. 1 Half-Duplex Drop-And-Insert Configuration Using DS1 Receiver 1 And DS1 Transmit 1

To set-up this test mode, proceed as follows.

1. Patch the DS1 Receiver 1 PCM Input jack to the DSX-1 MON jack as shown and set the INPUT SEL switch to MON.
2. Select the system format as required (with the SYST key/menu) and observe that all LED's in the 440B DS1 Receiver 1 section are off. If this is not the case, the source of trouble should be investigated before proceeding.
3. Depress momentarily the THRU 1 key in the DS1 Transmit 1 section and observe that the DIS'D LED is lit. At this point, the signal available at the T1 output jack in the DS1 Transmit 1 section contains an exact replica of the bit stream monitored by the DS1 Receiver 1 section; all 24 channels are passing through the test set as if it were a metallic connection.
4. Patch the DS1 Transmit 1 T1 Output jack to the DSX-1 IN jack and simultaneously insert a 100 Ohm terminating plug into the DSX-1 OUT jack as shown in fig 1. The insertion of the 100 Ohm termination is necessary to avoid waveform distortion as the line is no longer terminated by the bank when the 440B output is patched to the IN jack. (*)
5. In the DS1 Transmit 1 section, select the desired DS0 channel number.
6. Select the SIG BIT menu to display the signaling states in all 24 channels to check that the channel you want to preempt (insert) is idle.
7. If the channel is idle depress the SET key in the DS1 Transmit 1 section. This causes the DIS'D LED to turn off and the DS0 channel to be preempted. At this point, the content of 23 DS0 channels in the PCM bit stream delivered by the 440B to the channel bank is unchanged; the content of the selected DSO channel can be arbitrarily chosen as required.

Detailed information for selecting the content of the preempted channel is provided by sections 10 through 13 of this manual.

(*) Such termination plugs can be obtained from T-COM by ordering the following part numbers :

- 1694-004 : 310 type plug
- 1694-005 : Bantam type plug

To ensure against inadvertent disruptions of the traffic while in the THRU 1 mode, the 440B prevents you from :

- exiting without first depressing the THRU 1 key (the DS1 #1 key must be depressed within 700 ms of the THRU 1 key depression to exit the THRU/drop-and-insert mode)
- inserting the YEL ALM
- changing the line format (this format is the same as the format of the signal monitored by the DS1 Receiver 1 to ensure transparency).
- affecting the content of any DS0 channel when changing the DS0 channel No. selection. Whenever the channel No. is changed, the DIS'D LED turns on to indicate that the selection is not active. To activate the selection just depress momentarily the SET key.

As noted above, it is also possible to set-up the drop-and-insert mode using instead the combination of the DS1 Receiver 2 with the DS1 Transmit 2. This configuration is illustrated by figure 2 below. In practice, this second mode is seldom used by itself as it offers much less flexibility than the mode just described. A practical application of this mode is the test of echo cancellers as described in paragraph 15.5.3. This mode is also used jointly with the first mode to yield the full duplex drop and insert configuration.

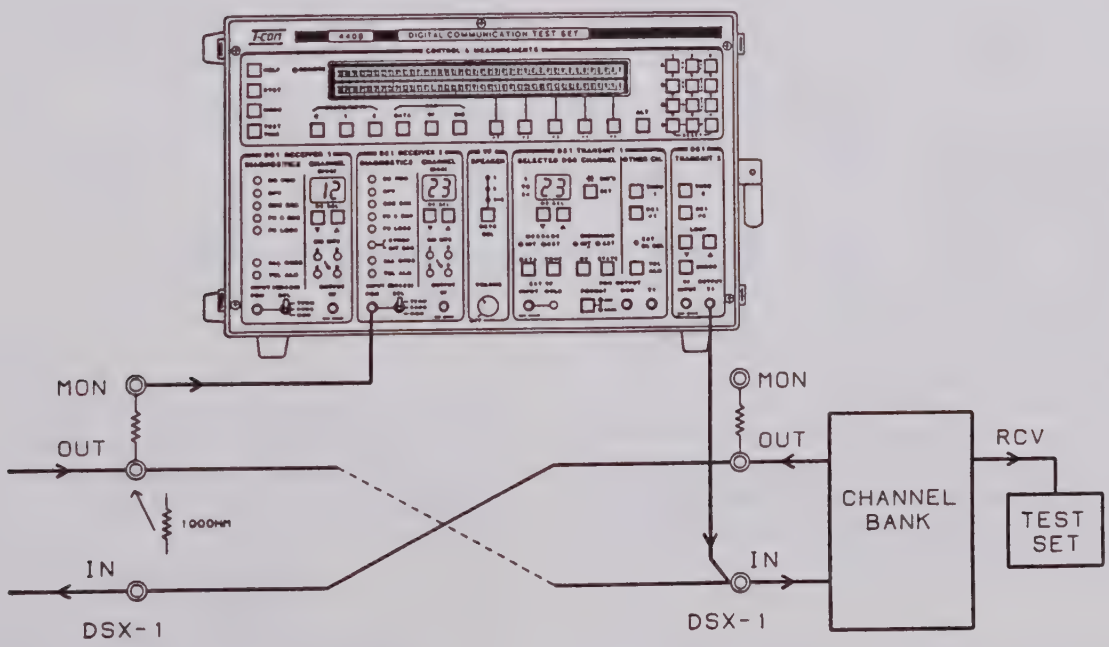


Fig. 2 Half-Duplex Drop-And-Insert Configuration Using DS1 Receiver 2 And DS1 Transmit 2

To set-up this test mode, proceed as follows.

1. Patch the DS1 Receiver 2 PCM Input jack to the DSX-1 MON jack as shown and set the INPUT SEL switch to MON.
2. Select the system format as required (with the SYST key/menu) and observe that all LED's in the 440B DS1 Receiver 2 section are off. If this is not the case, the source of trouble should be investigated before proceeding.
3. Depress momentarily the THRU 2 key in the DS1 Transmit 2 section to set the drop-and-insert mode. This key entry is accompanied by the display of the screen below.

```
CHANNEL SELECTION
                    DISABLED    ENABLED
active softkeys ------->    *           *
```

   The DISABLED header is underlined indicating that the DS0 channel selection is not active. At this point, the signal available at the T1 output jack in the DS1 Transmit 2 section contains an exact replica of the bit stream monitored by the DS1 Receiver 2 section; all 24 channels are passing through the test set as if it were a metallic connection.
4. Patch the DS1 Transmit 2 T1 Output jack to the DSX-1 IN jack and simultaneously insert a 100 Ohm terminating plug into the DSX-1 OUT jack as shown in fig 1. The insertion of the 100 Ohm termination is necessary to avoid waveform distortion as the line is no longer terminated by the bank when the 440B output is patched to the IN jack.
5. In the DS1 Receiver 2 section, select the desired DS0 channel number. This selection controls both the monitored (drop) channel selection and the preempted (insert) channel selection.
6. Select the SIG BIT menu to display the signaling states in all 24 channels to check that the channel you want to preempt (insert) is idle.
7. If the channel is idle, depress momentarily the ENABLE softkey. This causes the underline to migrate to this header and the preemption of the selected DS0 channel. At this point, the content of 23 DS0 channels in the PCM bit stream delivered by the 440B to the channel bank is unchanged; the content of the selected DS0 channel is the digitally encoded VF signal (if any) presented to the DS1 Transmit 2 VF input jack.

To ensure against inadvertent disruptions of the traffic while in the THRU 2 mode, the 440B prevents you from :

- exiting without first depressing the THRU 2 key (the DS1 #1 key must be depressed within 700 ms of the THRU 2 key depression to exit the THRU/drop-and-insert mode)
- inserting the LOOP UP or the LOOP DN codes

FULL-DUPLEX DROP-AND-INSERT TEST CONFIGURATION

15.4 This configuration is the combination of the two previously described ones. It is illustrated in figure 3 on the following page.

In this configuration, the 440B DS1 transmit 1 is set to the THRU 1 mode and the DS1 Transmit 2 is set to the THRU 2 mode. The 440B is set-up as previously described for the two half-duplex test configurations.

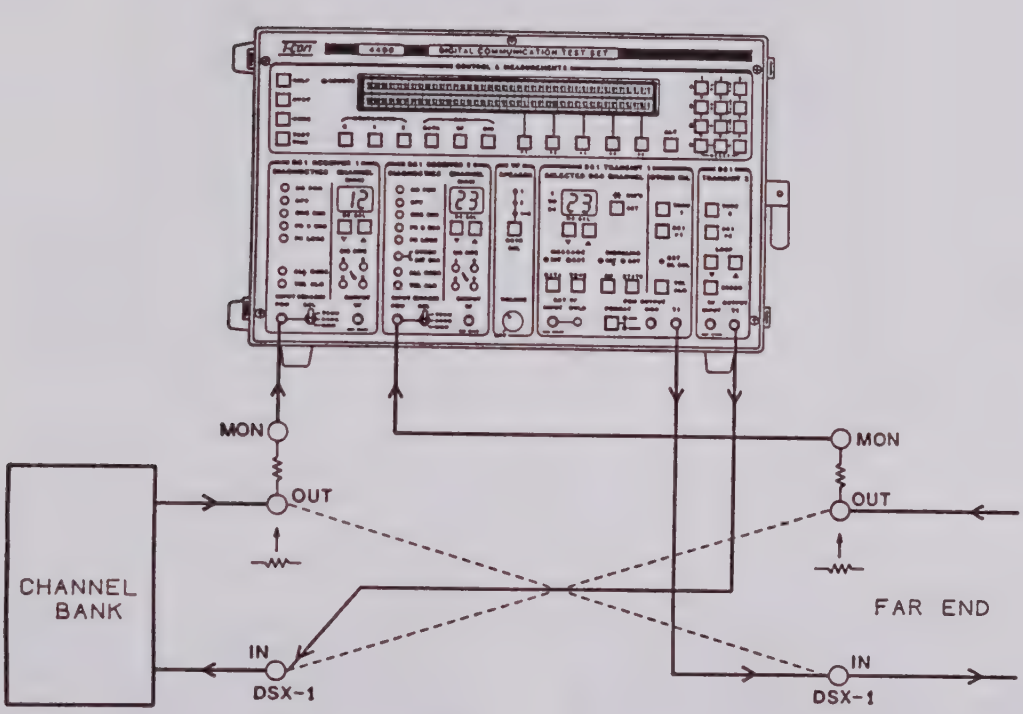


Fig. 3 Full-Duplex Drop-And-Insert Test Configuration.

APPLICATIONS

15.5 A few variations on the basic half-duplex drop-and-insert test configuration have interesting and useful applications. It is the purpose of this paragraph to briefly review the following applications :

- single DS0 channel loop back
- double-feeding a DS0 channel
- echo canceller characterization
- full duplex drop-and-insert trunk testing
- drop-and-insert dial/talk

SINGLE DS0 CHANNEL LOOP BACK

15.5.1 This configuration is useful to let the sender verify that the signal it sends in a DS0 channel is correct without having to disrupt the transmission in the other 23 channels. The use of the option 03 in the 440B allows you to accomplish this without in any way affecting the content of the looped back DS0 channel.

This configuration is illustrated in figure 4 on the following page.

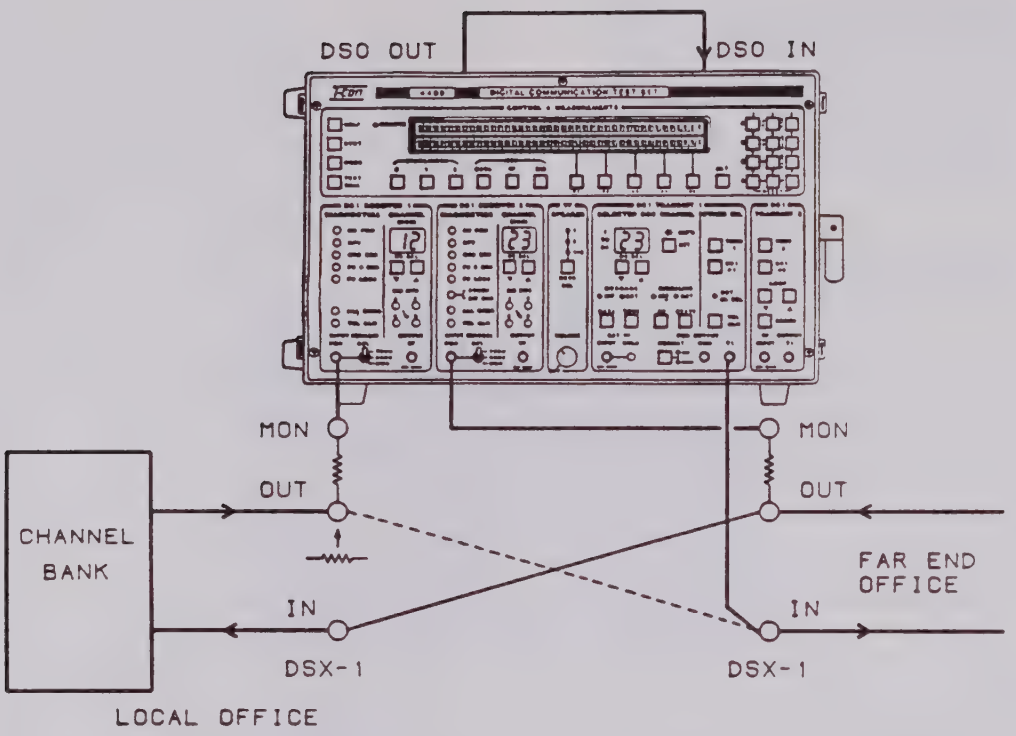


Fig. 4 DS0 Channel Loop Back Configuration

In this configuration the THRU 1 mode is implemented and the content of channel 23 monitored by the DS1 Receiver 2 is delivered as a 64 kb/s bit stream on the DS0 Data Channel Interface Output jack. By letting the DS1 Transmit 1 DS0 channel input selection be DATA and patching the DS0 Data Channel Interface OUTPUT jack to the INPUT jack, the 64 kb/s bit stream recovered from the DS1 Receiver 2 preempts the content of the selected DS0 channel in the Transmit 1 section. Consequently, the content of the DS0 channel monitored by the DS1 Receiver 2 is returned to the far-end office.

It should be noted that it is not required for the DS0 channel selection in the DS1 Receiver 2 and the DS1 Transmit 1 to be the same. If they are not the same, transposition is taking place.

Remark
To let the DS0 Data Interface deliver the content of the selected channel from the bit stream monitored by the DS1 Receiver 2, the DS1 Receiver 2 selection must be made in the DS0 DATA menu.

DOUBLE-FEEDING A DS0 CHANNEL

15.5.2 This configuration provides for duplicating the content of a DS0 channel in a DS1 bit stream into a second DS0 channel. This enables you to compare the operation of two decoder circuits in real-time. An exact duplication of the DS0 channel content is obtained by using the optional DS0 Data Access Interface (option 03).

This configuration is illustrated in figure 5 on the following page.

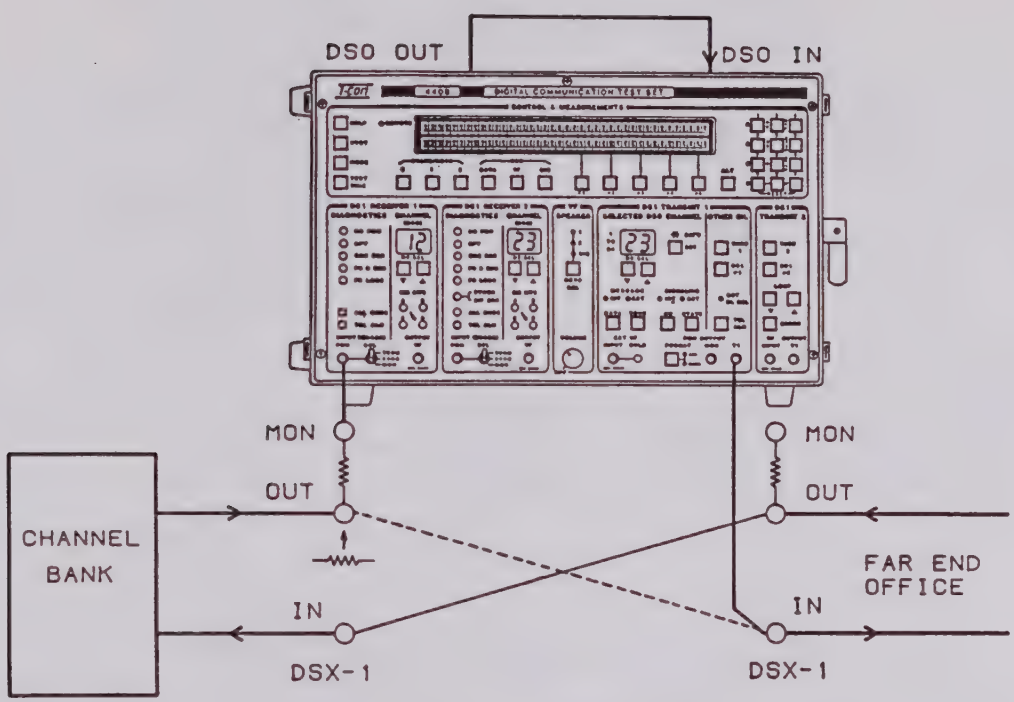


Fig. 5 Configuration For Double Feeding A DSO Channel

In this configuration the THRU 1 mode is implemented and the content of channel 12 monitored by the DS1 Receiver 1 is delivered as a 64 kb/s bit stream on the DS0 Data Channel Interface Output jack. By letting the DS1 Transmit 1 DS0 channel input selection be DATA and patching the DSO Data Channel Interface OUTPUT jack to the INPUT jack, the 64 kb/s bit stream recovered from the DS1 Receiver 1 preempts the content of the selected DS0 channel in the Transmit 1 section. In this example, the T1 bit stream delivered by the DS1 Transmit 1 carries the same pattern in channels 12 and 23.

Since the channel number selection is arbitrary, the content of any channel in the monitored bit stream can be duplicated in any other channel in the outgoing bit stream.

Remark
To let the DS0 Data Interface deliver the content of the selected channel from the bit stream monitored by the DS1 Receiver 1, the DS1 Receiver 1 selection must be made in the DS0 DATA menu.

ECHO CANCELLER CHARACTERIZATION

15.5.3 While a great many tests can be carried-out to evaluate the performance of DS1 echo cancellers, perhaps the most important is to verify the signal cancellation effectiveness as a function of the signal level, its frequency and the transmission properties (including loss and delay) of the transmission medium. A basic test set-up required to perform this characterization is illustrated by figure 6.

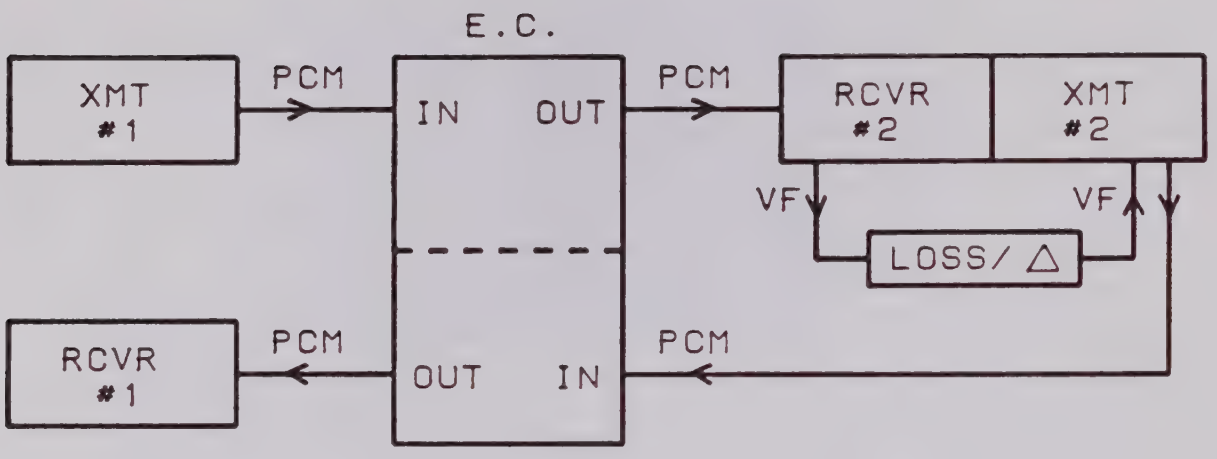


Fig. 6 Basic Echo Canceller Test Configuration

In this figure, the XMT 1 signal source supplies to the echo canceller a DS1 formatted bit stream in which all DS0 channels may be idle except for the one under test which typically contains a calibrated VF tone. The echo canceller processes this signal and delivers the modified DS1 signal to RCVR 2. This RCVR decodes the content of the selected DS0 channel and supplies the reconstructed VF signal to an artificial line. This line simulates the transmission loss and delay introduced by the transmission medium and yields a signal representing the echo.

The echo signal is digitally encoded and inserted into a selected DS0 channel by the XMT 2. The DS1 signal delivered by the XMT 2 is processed by the second half of the echo canceller. In turn, the echo canceller delivers a modified version of this signal to the RCVR 1. This RCVR decodes the content of the selected DS0 channel and measures the signal or noise level in this channel.

By comparing the level of the signal received with the level sent and factoring in the loss introduced by the artificial line, you can obtain a family of graphs showing the relationship between signal level, signal frequency, transmission medium loss and transmission delay as all these parameters are easily changed in the set-up.

By using an artificial line along with the 440B, the basic test configuration can be obtained. This is illustrated in figure 7 on the following page.

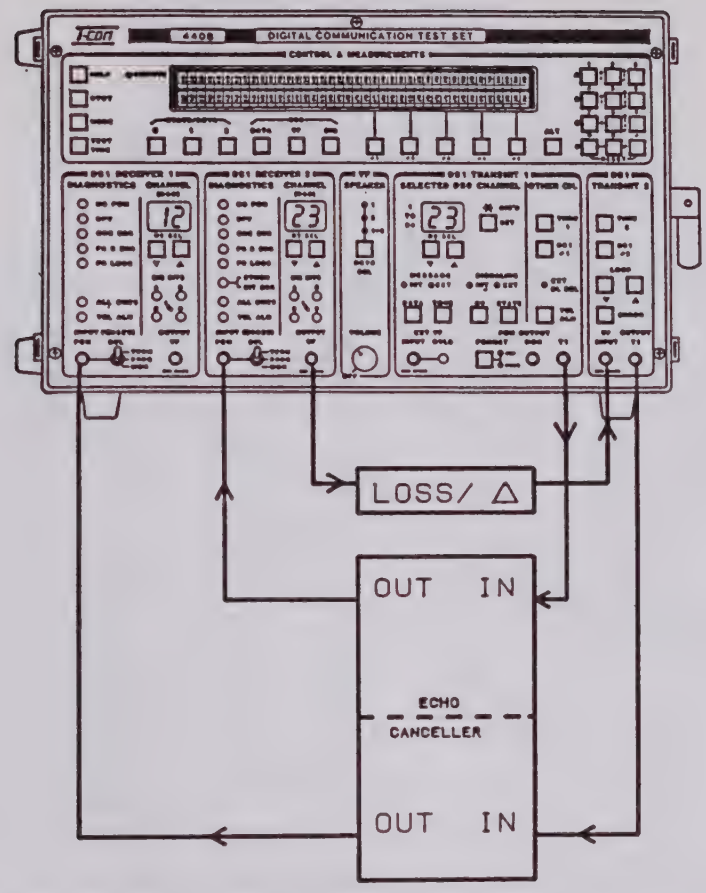


Fig. 7 Configuring the 440B to test a DS1 Echo Canceller

In figure 7 all DS0 channel selections are the same since the test is performed on a two-way transmission path. The DS1 Transmit 1 inserts a TONE with the desired level and frequency in the selected DS0 channel while the other channel content is set to IDLE. The DS1 Transmit 2 is set to the THRU 2 mode. Finally, in the CONTROL & MEASUREMENTS section the DS0 VF key should have the FLOSO state as the VFDT should yield either the measure of the echo signal or noise level.

Full Duplex Drop & Insert Trunk Testing

15.5.4 The full duplex drop-and-insert mode is required when it is necessary to condition the non-test direction of a circuit in the busy (off-hook) or idle (on-hook) state while performing tests in the other direction.

In this configuration, both directions of the T1 facility are connected to the 440B as shown in figure 3. Be sure to connect the transmitter 1 output to the DSX jack associated with the side of the switch receiving the outpulsed digits. The transit side of the switch which returns wink or dial tone should be connected to RECEIVER 2 input.

When performing drop-and-insert testing on a circuit in a working trunk group it is often necessary to condition the non-test direction either idle or busy. In many cases an off-hook condition toward the closed end of an FX circuit causes a permanent ring. This condition is avoided by setting the signaling on-hook toward the closed end (non-test direction) while testing toward the open end. Conversely, when testing toward the closed end, the open end (non-test) direction is set off-hook to prevent an in-coming call from going high and dry.

The rear panel ABCD switch S3 is used to set the required signaling state of the non-test direction using the channel selector in Receiver 2.

Drop-and-Insert Dial/Talk

15.5.5 The 440B can be used to initiate a dialing sequence on a selected channel and by connecting the T-COM 2889-001 Handset Adapter, as shown in Figure 8, the tester can talk and listen.

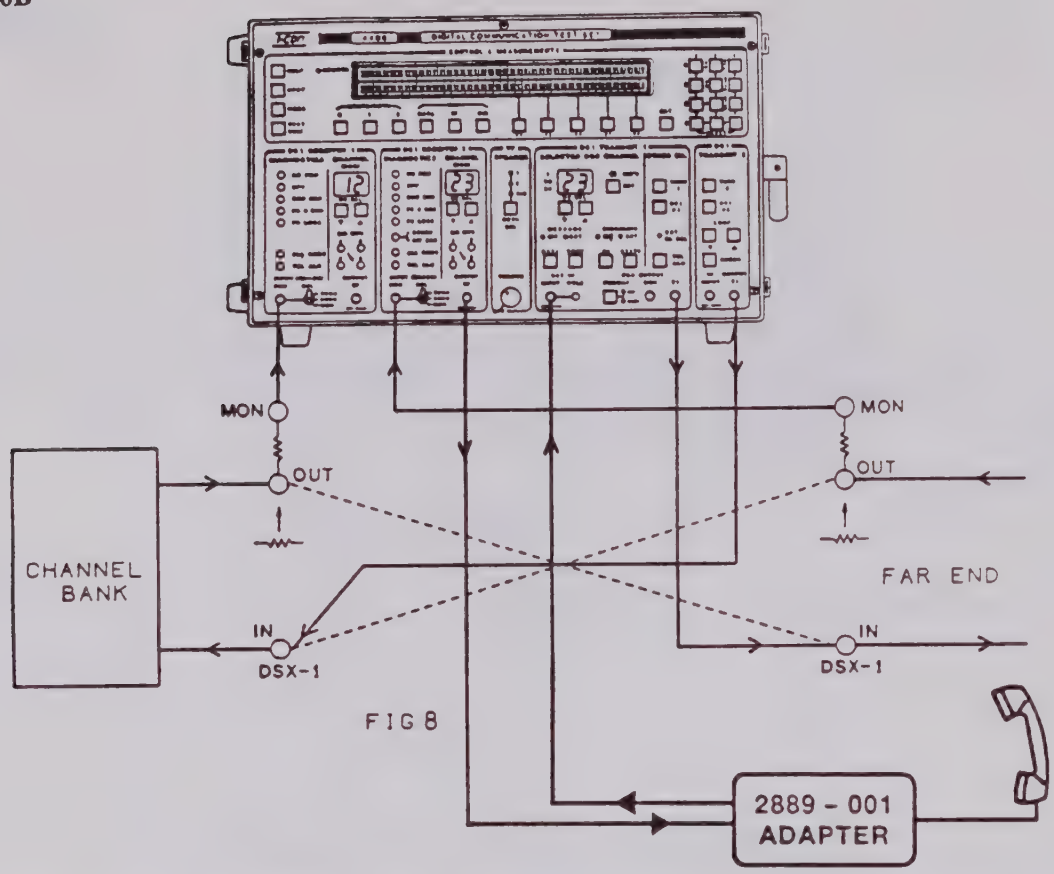


Fig. 8 Setting up the 440B in the D/I mode to provide VF communication with the far end

Call set-up procedure:

This procedure applies to the set-up illustrated in figure 8. Carry out the steps 1 through 7 in the order listed.

1. Place the 440B in the THRU 1 (drop- and-insert) mode.

2. Select the same channel number in both DS1 Receiver sections and in the Transmit 1 section.

3. Turn the volume level all the way down on the 440B to avoid acoustic interaction with the handset.

4. Momentarily depress the STATE key in the Transmit 1 section and set the signaling states for "off-hook" (normally A,B set to 1).

5. Momentarily depress the No. key in the Transmit 1 section and enter the telephone number of the operator at the far end. This number must always be preceded by the on-hook (↓) and off-hook (↑) symbols.

6. When the selected channel is idle, depress momentarily the SET key and then the GO softkey. This causes the stored telephone number to be dispatched. If the call is going through, when the number has been sent you should hear either the ring back tone or the busy signal.

7. When the party at the other end answers, momentarily depress the TONE key in the Transmit 1 section. At this point, the talk path is established.

16. OUT OF SERVICE TESTING

INTRODUCTION

16.1 The out-of-service testing capability is provided only when the 440B is equipped with option 05. This capability is primarily intended to characterize the transmission integrity of a facility. In this chapter, you will find:

- a description of the out-of-service testing principle
- a description of the 440B out-of-service testing capabilities
- directions for setting-up the 440B to perform out-of-service testing

If the 440B is not equipped with option 05, the content of this chapter is of limited application to the operation of the instrument.

OUT-OF-SERVICE TESTING PRINCIPLE

16.2 When testing a PCM transmission facility in an out-of-service basis, the transmission facility cannot carry the normal traffic. Instead the facility carries exclusively a test pattern intended to either simulate the normal traffic or to stress the transmission equipment. At the same time, a PCM transmission monitoring circuit analyzes the PCM patterns at any access point along the transmission facility to detect the occurrence of transmission bit errors over time and can thus compute the average bit error rate for the facility.

The above described method requires two separate test sets: one sender and one monitor. When the transmission facility can be looped at the far end, either via a remote loopback circuit or perhaps a simple patch cord, it is also possible to perform the test with a single test set such as the 440B which includes both the PCM test pattern sending and monitoring capabilities.

Regardless of the testing configuration, the PCM monitor circuit detects errors by comparing on a bit-by-bit basis the monitored pattern with a perfect copy of the signal delivered by the sender to the facility. This copy is created by a generator similar to the one used by the sender. This generator is synchronized with the monitored pattern to ensure proper phase relationship. This phase relationship is required to obtain a meaningful bit-by-bit comparison.

Typical patterns used to simulate traffic consist of relatively random bit sequences. These sequences are generally referred to as quasirandom or pseudorandom because they have a finite length and must be repeated over time. Consequently, unlike real traffic, they are not truly random. Examples of such patterns are given in table 16.1.

Name	Length	Comment
2^{15}-1	32,767	14 consecutive zeros max
2^{20}-1	1,048,575	19 consecutive zeros max
2^{20}-1	1,048,575	14 consecutive zeros max (QRS)
2^{23}-1	8,388,607	22 consecutive zeros max

Table 16.1 Commonly used PRBS test patterns

In addition to patterns simulating traffic, other test patterns are used for stressing the transmission facility. Such patterns include 3/24 (three ones spread in a 24 bit sequence), 1/8 (one followed by seven zeros). As in the case previously described, the monitoring circuit performs bit-by-bit comparison with a copy of these patterns.

The measurement of the average bit error rate (BER) is obtained by calculating the ratio of the total number of bit errors detected to the total number of bits transmitted. This second number is obtained from the product of the nominal bit rate (1,544,000 bits/sec) by the elapsed test time expressed in seconds.

The out-of-service testing method is very powerful to verify quickly that a transmission facility is suitable for carrying the intended PCM traffic. This is a particularly useful test when a new installation has been completed and must be verified prior to placing it into service. The out-of-service test method is not useful to evaluate the performance of a channel bank.

440B OUT-OF-SERVICE TESTING CAPABILITIES

16.3 When equipped with option 05 the 440B is capable of performing all the measurements described in the preceding section and a few additional ones.

The out-of-service test pattern sending capability is associated with the DS1 Transmit 2 section. This section can generate all the test patterns described in the preceding paragraphs and some additional test patterns as well: a 24-bit user-defined stress pattern and miscellaneous loop codes for controlling the remote looping feature of CSU's, NI's (network interface units) as well as other devices. Furthermore, the DS1 Transmit 2 has a provision for injecting various impairments in the delivered bit streams.

The bit monitoring capability is provided exclusively by the DS1 Receiver 2. This receiver is always primed to compare the monitored PCM with the pattern delivered by the DS1 Transmit 2 section when this pattern is not channelized. The DS1 Receiver 2 displays in real time the pattern synchronization (SYNC) as well as each occurrence of a bit error. A bit error can be detected only while pattern synchronization prevails. The detected bit errors and the synch loss-seconds are counted and the BER computation is performed by a dedicated microcontroller.

Because the DS1 bit error counting period is often specified by company practices, the 440B is equipped with a settable test timer. This feature enables you to limit the test time to any period bounded by the interval of 1 minute to 100 hours.

> **Note:**
> If the 440B is not equipped with option 05, the instrument can still generate all the loop codes, the all-ones and the 1/8 patterns.

The next section describes how to set-up the 440B for performing out-of-service testing.

SETTING-UP THE 440B FOR OUT-OF-SERVICE TESTING

16.4 To perform out-of-service testing, you may use the 440B to send test patterns, to monitor them or to perform both functions at the same time. These functions are discussed separately below.

SETTING-UP THE SENDING FUNCTION.

16.4.1 You may set the DS1 Transmit 2 to deliver either some loop codes or some test patterns. To send a test pattern, you need to momentarily depress the DS1 #2 key. This depression causes the FLOSO state to be transferred to this key and the VFDT to display a screen similar to screen [1] below.

Screen [1]

DS1	3/24	PRBS	CODE	ALL 1's		
#2	1/8	CHANNELIZED			< >	ENTR

In the screen [1], the CHANNELIZED heading is underlined (not shown). The momentary depression of either pointer softkeys allows you to place the underline at either heading location. When the CHANNELIZED heading is underlined and the ENTR softkey is depressed, screen [2] is displayed.

Screen [2]

DS1	IDLE	1005Hz/-20dBm0		ALT
#2			< >	SEL

The IDLE heading is underlined (not shown). The underline may be moved to the other selection by depressing momentarily either pointer softkey. When the ALT SEL softkey is momentarily depressed, screen [1] is displayed anew.

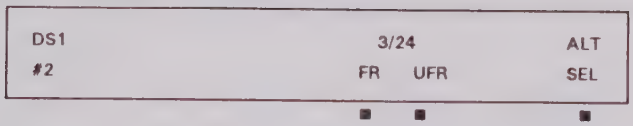
When the 440B is equipped with option 05, any selection in screen [1] can be active. If the option 05 is not installed, the selection of 3/24, PRBS and CODE cannot be activated. In this case, the depression of the ENTR softkey causes the screen [3] to appear.

Screen [3]

DS1	Option 05 is not installed	ALT
#2		SEL

By momentarily depressing the ALT SEL softkey, screen [1] is displayed anew. If option 05 is installed and the heading 3/24 is underlined when the ENTR key is depressed in screen [1], screen [4] is displayed.

Screen [4]



Either the FR or the UFR heading in screen [4] is underlined to indicated that the selected pattern is either framed or unframed. This selection is changed by depressing the softkey whose heading is not underlined. By momentarily depressing the ALT SEL softkey, screen [2] is displayed anew.

If in screen [2] the heading 1/8 is underlined when the ENTR key is depressed, screen [5] is displayed.

Screen [5]

Either the FR or the UFR heading in screen [5] is underlined to indicated that the selected pattern is either framed or unframed. This selection is changed by depressing the softkey whose heading is not underlined. By momentarily depressing the ALT SEL softkey, screen [2] is displayed anew.

If in screen [2] the heading ALL 1's is underlined when the ENTR key is depressed, screen [6] is displayed.

Screen [6]

Either the FR or the UFR heading in screen [6] is underlined to indicated that the selected pattern is either framed or unframed. This selection is changed by depressing the softkey whose heading is not underlined. By momentarily depressing the ALT SEL softkey, screen [2] is displayed anew.

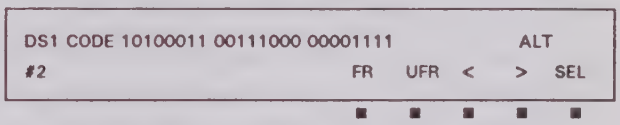
If option 05 is installed, and the heading QRS in screen [2] is underlined when the ENTR key is depressed, screen [7] is displayed.

Screen [7]

The current selection is underlined [not shown]. With the use of the < and > softkeys you can move the underline to change the selection. The operation of this screen is entirely consistent with previously described screens. The FR/UFR selection is changed by depressing the softkey whose heading is not underlined. By momentarily depressing the ALT SEL softkey, screen [2] is displayed anew.

If option 05 is installed, and the heading CODE in screen [2] is underlined when the ENTR key is depressed, screen [8] is displayed.

Screen [8]



Screen [8] displays the current code. This code can be arbitrarily set by the user and extend over 8, 16 or 24 consecutive bits. Any code can be edited with the 0 and 1 numeric keys in the keypad. To shorten the code to 8 bits, you must enter the * in the 9th bit position. When this is entered, all the bit positions on the right side of the * are blanked-out. This may be undone by entering a 1 or a 0 in the 9th bit position. When this is undone, all the bit positions on the right take the value 0. The same concept is extended to 16 bit codes by setting the * in the 17th bit position. The use of the < and > softkeys can speed-up the editing process. When the FR softkey is underlined, the generated bit stream consists of a framed sequence in which the content of the first three channels is defined respectively by the content of the first, second and third byte. The content of these first three channels is repeated 7 more times to yield a total of 24 channels. When the UFR softkey heading is underlined, the 24-bit pattern repeats itself endlessly. If the ALT SEL softkey is depressed in screen [8], screen [2] is displayed anew.

Error injection

Except when a loop code is being delivered by the DS1 Transmit 2 section, you can always inject some errors in the outgoing DS1 bit stream. To this end, the momentary depression of the ERROR key causes

the FLOSO state to be transferred to this key and the VFDT to display the screen [9] below.

Screen [9]

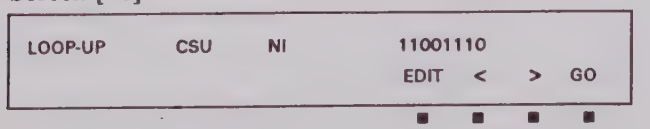
The current selection is underlined [not shown]. By depressing either the < or the > softkey, the underline can be moved under the desired selection. In screen [9] the presence of the headings for FR BIT, CRC and BIT is conditional. The FR BIT heading appears only if the sequence selected in the DS1 #2 menu is framed. The CRC heading appears only if the sequence selected in the DS1 menu is framed AND the current SYSTem selection is ESF.

The momentary depression of the GO softkey causes the activation of the underlined selection and this is reflected by the flashing of the selection. While the selection flashes, the corresponding impairment is introduced at the rate of 5 per second. This condition prevails until either the STOP softkey or the SNGL (single event) softkey is depressed. The underline impairment can be injected once for each depression of the SNGL softkey.

LOOP UP/DN selection

The loop-up and loop-down code sending capabilities are nearly identical and, for simplicity, only the loop-up code selection is described in details. The only differences between the two functions concern the actual codes generated and the corresponding screen headings. Unless the THRU 2 selection is active (THRU 2 key is lit), the depression of either key pre-empts the VFDT. If the THRU 2 mode does not prevail and the LOOP UP key is depressed, a screen similar to screen [10] is displayed.

Screen [10]



The current selection is underlined [not shown]. With the use of the < and > softkeys you can move the underline to change the selection. The EDIT softkey heading appears only if the byte is underlined. The underlined LOOP code is generated by the Transmit 2 circuitry while the GO softkey is depressed and for 5 seconds thereafter even if another menu is accessed. The only situation causing the immediate stop of the LOOP code generation is when the THRU 2 key is depressed.

The user-defined code can be edited to represent any binary code having up to 8 bits in length. When the EDIT key is momentarily depressed, a screen similar to screen [11] is displayed.

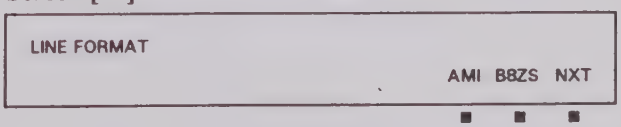
Screen [11]

In screen [11] the pointer softkeys can be used to move the flashing underline (not shown) to the desired bit position. The bit at that position can be set to 1 or 0 by depressing the appropriate key on the keypad. If the pattern is to have fewer than 8 bits, the BLNK softkey can be used to clear the location with the flashing underline as well as all positions on its right. The selection becomes effective and is stored in the battery powered memory only when the ENTR softkey is depressed.

Line format selection

When the 440B is operated in the stand alone mode, the line format can be set to either AMI or B8ZS. This selection is obtained by depressing the DS1 #2 key twice. When this is done, a screen similar to screen [12] is displayed.

Screen [12]



The current selection is underlined (not shown). It can be changed by depressing the softkey for the alternate selection. The depression of the NXT softkey causes the exit from the line format selection screen.

When operated in the THRU 2 mode, the Transmit #2 AMI/B8ZS format selection is unconditionally controlled by the format detected by the RCVR #2.

SETTING-UP THE DS1 MONITORING FUNCTION.

16.4.2 The out-of-service monitoring capability in the 440B is completely automatic. In effect, the pattern selection for the comparison required in the bit-by-bit check is performed simultaneously with the setting of the DS1 Transmit 2 selections. The access to the collected data is obtained by simply paging through the STATS/RCVR 2 menu. Page 4-4 in this manual contains an illustration of the BER screen obtained when the option 05 is installed in the 440B.

To set a time limit to the duration of an out-of-service (as well as an in-service) test, the 440B provides a user settable test timer. The use of this capability is described on page 3-4.

17. PRINTER INTERFACE PORT

INTRODUCTION

17.1 When equipped with option 04, the RS-232-C interface provided on the instrument rear panel is active and can be used for interfacing a printer or a terminal with the 440B. This capability is primarily intended to enable the downloading of the impairment statistics acquired by the 440B alone or along with its add-on modules. This capability is independent of the remote control feature described in the next chapter. In this chapter, you will find:

- a description of capabilities provided by the RS-232-C port
- a description of RS-232-C port interface
- directions for using the RS-232-C interface capability

If the 440B is not equipped with option 04, the content of this chapter is not applicable to the operation of the instrument.

RS-232-C PORT INTERFACE CAPABILITIES

17.2 The impairment data obtained and processed by the 440B can be transferred via the RS-232-C port to various equipment compatible with this interface standard. This includes primarily printers and PC type terminals. The connection to this equipment can be performed either by cable or via a modem. When the 440B is equipped with the option 53A or 52B, the impairment data obtained from these add-on units is down-loaded automatically along with the data obtained by the 440B proper. The use of a printer with keyboard or a terminal extends the usefulness of the interface by letting the user obtain information on demand and to provide a limited remote control capability.

The data delivered by the RS-232-C port is completely formatted and can readily be displayed by a standard 80-column line printer or a dumb terminal. To ease the operation and to reduce the need for reference to this manual, a command screen is available and access information is automatically supplied at the start of a session. The message downloaded by the 440B following power-up of the 440B is reproduced below.

```
 T-COM 440B DS1 COMMUNICATION TEST SET
(*) WITH OPTION 53A
    (DS1C/DS1 MONITOR/DEMULTIPLEXER)
(*) WITH OPTION 52B
    (DS3/DS2/DS1 MONITOR/DEMULTIPLEXER)
 - SELF CHECK OK
 - DATE : ab/cd/ef  <M/D/Y>
 - TIME : gh:ij     <HH:MM>
 - TYPE H <cr>  FOR COMMAND
                  INFORMATION
                  (cr = enter key)
```

The (*) is not included, it is used here to flag that the line is supplied only if applicable.
When the command H <cr> is received from the terminal, the RS-232-C microcontroller delivers the message on the following page:

The lines starting with the (%) are included only if the 440B is equipped with option 52B. As noted from the command listing, you can unconditionally reset the instrument from the keyboard and to obtain a summary report. When the 440B is equipped with the 52B, you may also select the demultiplexed DS1 group number and request the number of the demultiplexed DS1 group selection.

The receipt of a RESET command by the 440B causes the clearing of all the impairment counters and resets both the elapsed test timer and the 52B option if installed.

The receipt of the S command by the 440B causes the instrument to download the most current summary report. The format of this report depends on the 440B configuration and it is illustrated in this section.

Time and date stamped transmission impairment events are captured during a sequence of discrete time periods. The time period is user-selectable in the range of 1 to 99 minutes; it is set from the terminal or printer keyboard by entering the command: /10 if the desired download resolution is 10 minutes. The longer the selected download period, the shorter the length of the printout in the event of a severely impaired transmission.

All events collected during a discrete time period are printed at once in the most efficient manner. For example, if 3 BPV's occurred during this period, a

single line item is downloaded indicating this occurrence, not three distinct line items.

COMMANDS	DESCRIPTIONS
RESET<cr>	Clears all impairment counters and resets the elapsed test timer.
S<cr>	Causes the downloading of the most current summary report.
/mn <cr>	Sets the activity report time period to the value mn in minutes (Range 1-99).
(%) RESET/mn <cr>	Selects the DS1 group No mn. The value mn must be in the range 1 through 28. Whether the group No is changed or not, this entry always clears all impairment counters and resets the elapsed testtimer.
(%)	
(%)	
(%) ?<cr>	Causes the downloading of the current DS1 group No selection.
H <cr>	Causes the downloading of this help message.

NOTES : <cr> : Return (RTN) or ENTER key entry.

While a message is being downloaded to the terminal, key entries are ignored.

Three tabulation formats are used to accommodate the cases for:
- 440B by itself
- 440B equipped with option 53A and
- 440B equipped with option 52B

These three tabulations are illustrated in figure 17.1 through 17.3 at the end of the chapter.

In addition to the impairment statistics normally captured by the 440B, the downloading also includes the state of the AIS, remote alarm and whether a plug is inserted in various PCM input jacks. This last information is quite useful to ensure the validity of the impairment measurement. Several symbols are used as listed in table 17.1. to represent these conditions.

- S for SET
- C for CLEAR
- S/C for SET then CLEAR (when during the same minute the function is set and cleared).
- OUT when plug is out
- IN when plug is in
- O/I for OUT then IN (when during the same minute, the plug is pulled-out and re-inserted).

Table 17.1 Event symbols listing

As previously noted, activity summary reports are downloaded whenever the ASCII character S is received (all by itself) by the RS-232-C controller. The downloading of the summary report does not cause any loss of data acquired while the downloading takes place. The format of these reports depends on the 440B configuration. Inapplicable line items are simply omitted when the format selection does not call for certain parameters (i.e. ESF & C-BIT). The three summary report formats available are illustrated in figures 17-4 through 17-6 at the end of the chapter.

RS-232-C PORT INTERFACE DESCRIPTION

17.3 The RS-232-C interface port consists of a D-SUB 25 position female connector. The active pins on this connector are listed and described in table 17.2. on the following.

Pin No.	Identifier	Description
1	FG	Protective Ground (frame)
2	TD	Transmitted Data (out)
3	RD	Received Data (in)
4	RTS	Request to Send (out)
5	CTS	Clear to Send (in)

continued

Pin No.	Identifier	Description
6	DSR	Data Set Ready (in)
7	SG	Signal Ground (common return)
20	DTR	Data Terminal Ready (out)
All Others		Not used

Table 17.2 RS-232-C Connector Pin Assignment

Notes:

All data leads on this connector adhere to the state convention:
"zero" = +10 V nominal, "one" = -10 V nominal

The data is formatted as follows : 7-bit, no parity, 2 stop bits.

The baud rate is controlled by the setting of the rear panel switch S4 position 2, 3 and 4 as listed in table 17.2.

Rate	S4/4	S4/3	S4/2
300	ON	ON	ON
1200	ON	ON	OFF
2400	ON	OFF	ON
4800	ON	OFF	OFF
9600	OFF	ON	ON

Table 17.3 Baud Rate Selection

USING THE RS-232-C INTERFACE PORT

17.4 To download the transmission statistics processed by the 440B, the RS-232-C port must be patched to a terminal either directly or via a modem and a transmission line.

The terminal may be either a plain 80-column line printer providing the receive-only function, a printer with a keyboard providing both send and receive or a computer. In any event, the terminal must be equipped with an RS-232-C serial interface port configurable as follows:

- baud rate: any value in the sequence 300, 1200, 2400, 4800 or 9600
- format : ASCII 7 bits, no parity, 2 stop bits

The interconnecting cable between the 440B and the terminal must have the null modem configuration. An example of the null modem cable used for interconnecting the 440B to a TI model 703 is given in figure 17.7.

When interfacing the RS-232-C with a modem, only the baud rate must be compatible with the selected baud rate on the 440B. The interconnecting cable between the 440B and the modem requires straight connection for all the leads listed in table 17.2.

Once properly connected to the 440B, the printer/terminal is ready to operate as described in section 17.2. One should note that access to the activity summary reports and to other commands requires a printer equipped with a keyboard.

For convenience, you may order from T-COM straight or null-modem configuration cables as well as the TI 703 printing terminal. Refer to chapter 24 for description and ordering information.

ACTIVITY REPORT DATE	TIME	EVENTS	DS1/DG1 COUNTS	DS1/DG2 COUNTS
ab/cd/ef	10:12	INPUT PLUG	IN	IN
ab/cd/ef	10:13	ERR-SEC	1	
		CRC ERR	1	
ab/cd/ef	10:52	FR BIT ERR		1

Fig 17.1 Activity report generated by a 440B not equipped with either option 53A or 52B

ACTIVITY REPORT DATE	TIME	EVENTS	DS1C COUNTS	DS1/DG1 COUNTS	DS1/DG2 COUNTS
ab/cd/ef	10:12	INPUT PLUG	IN	OUT	OUT
ab/cd/ef	10:13	ERR-SEC	1	1	1
		FR BIT ERR		1	
		CRC ERR			1
ab/cd/ef	10:52	FR BIT ERR	1	1	1

Fig 17.2 Activity report generated by a 440B equipped with option 53A

ACTIVITY REPORT DATE	TIME	EVENTS	DS3 COUNTS	DS2 COUNTS	DS1/DG1 COUNTS	DS1/DG2 COUNTS
ab/cd/ef	10:12	INPUT PLUG	IN			OUT
ab/cd/ef	10:13	ERR-SEC	1			
		PARITY ERR	1			
ab/cd/ef	10:52	FR BIT ERR	1	1		1

Fig 17.3 Activity report generated by a 440B equipped with option 52B

ACTIVITY SUMMARY

DATE : / / (M/D/Y) TIME : : (H:M)
TEST TIME : : (H:M)

EVENTS	DS1/DG1 COUNTS	DS1/DG2 COUNTS
INPUT PLUG	IN	IN
BPV	125	32
ERR-SEC	41	3
CRC ERR	12	3
FR BIT ERR	4	1
FR LOSS-SEC	1	1
AIS	1	0
REM ALARM	0	0
BIT ERROR	N/A	N/A
SYNC-LOSS-SEC	N/A	N/A
BER	N/A	N/A
FBER	3.2 E-8	*
CBER	3.6 E-8	*

* Insufficient No. of errors to obtain a reliable measurement.

********** END OF REPORT **********

Fig 17.4 Activity summary generated by a 440B not equipped with either option 53A or 52B

Note:
The Nos. for AIS and REM ALARM represent the number of times these events have been detected, not the number of seconds the condition prevailed.

ACTIVITY SUMMARY

DATE : / / (M/D/Y) TIME : : (H:M)
TEST TIME : : (H:M)

EVENTS	DS1C COUNTS	DS1/DG1 COUNTS	DS1/DG2 COUNTS
INPUT PLUG	IN	IN	IN
BPV	103	125	32
ERR-SEC	41	41	3
CRC ERR	N/A	12	3
FR BIT ERR	4	4	1
FR LOSS-SEC	1	1	1
AIS	1	1	0
REM ALARM	0	0	0
BIT ERROR	N/A	N/A	N/A
SYNC-LOSS-SEC	N/A	N/A	N/A
BER	N/A	N/A	N/A
FBER	7.1 E-7	3.2 E-8	*
CBER	N/A	3.6 E-8	*

* Insufficient No. of errors to obtain a reliable measurement.

********** END OF REPORT **********

Fig 17.5 Activity report generated by a 440B equipped with option 53A

ACTIVITY SUMMARY

DATE : / / (M/D/Y) TIME : : (H:M)
TEST TIME : : (H:M)

EVENTS	DS3 COUNTS	DS2 COUNTS	DS1/DG1 COUNTS	DS1/DG2 COUNTS
INPUT PLUG	N/A	N/A	OUT	IN
BPV	103	103	125	32
ERR-SEC	41	41	41	3
CRC ERR	N/A	N/A	12	3
PARITY ERR	14	N/A	N/A	N/A
C-PAR ERR	12	N/A	N/A	N/A
FEBE	32	N/A	N/A	N/A
FR BIT ER	12	6	4	1
FR LOSS-SEC	1	1	1	1
AIS	1	1	1	0
REM ALARM	0	0	0	0
BIT ERROR	N/A	N/A	N/A	N/A
SYNC-LOSS-SEC	N/A	N/A	N/A	N/A
BER	N/A	N/A	N/A	N/A
FBER	7.1 E-7	7.1 E-7	3.2 E-8	*
CBER	N/A	N/A	3.6 E-8	*
PBER	7.4 E-7	N/A	N/A	N/A
C-PBER	7.4 E-7	N/A	N/A	N/A
FEBEBER	4.4 E-6	N/A	N/A	N/A

* Insufficient No. of errors to obtain a reliable measurement.

********** END OF REPORT **********

Fig 17.6 Activity report generated by a 440B equipped with option 52B

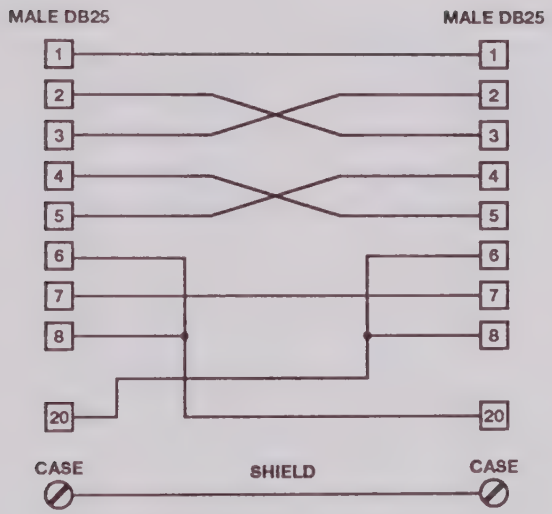


Figure 17-1. Null-Modem Cable Configuration

18. REMOTE CONTROL FEATURE

The 440B has been designed to accept an optional remote control feature. When this feature is released this section will provide the supporting documentation.

19. AUXILIARY ACCESS

INTRODUCTION

19.1 The 440B provides a number of timing signals intended for connecting auxiliary equipment. This section contains information necessary for using the 37 pin I/O DATA & TIMING ACCESS (J24) and the 9 pin SIG OUTPUTS connector (J19) provided on the rear panel.

37-PIN I/O DATA AND TIMING CONNECTOR

19.2 This interface is marked J24 on the rear panel. It provides access to the input/output data and timing circuits of the 440B. The information on each pin is given in Table 19.1.

All signals and status leads on this connector interface with high-speed CMOS logic circuits. When the load is purely capacitive and does not exceed 50 pF, the output logic levels are as specified below:

State	Level (Volts)
1	+5.0 ± 0.2
0	0.0 ± 0.2

Timing relationships between signals available on this connector are shown in Fig.19.1. In this figure, the clock period is 648 ns nominal with a duty cycle of 50% ± 5%. All signals are delayed with respect to the corresponding clock rising edge by 20 ns nominal.

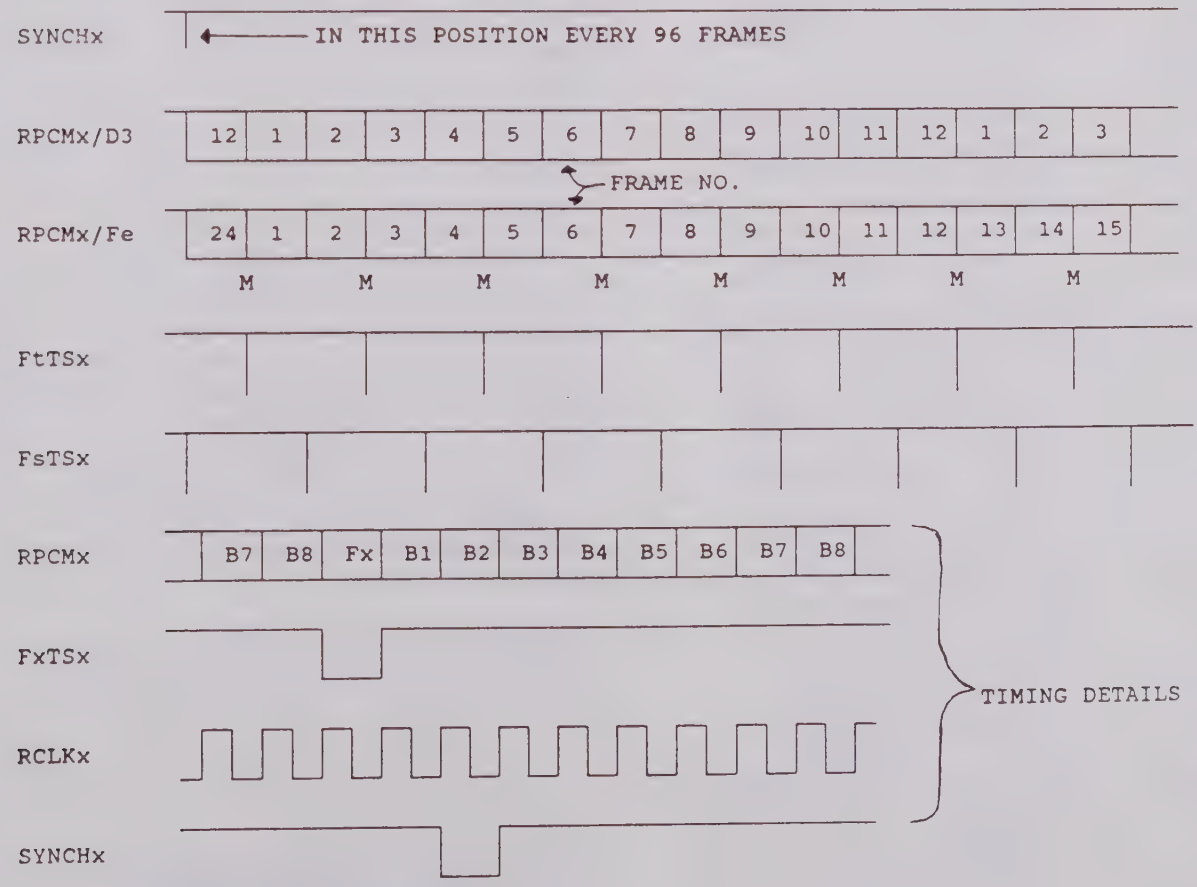

SYNCHx
IN THIS POSITION EVERY 96 FRAMES
RPCMx/D3
12 1 2 3 4 5 6 7 8 9 10 11 12 1 2 3
FRAME NO.
RPCMx/Fe
24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
M M M M M M M M
FtTSx
FsTSx
RPCMx
B7 B8 Fx B1 B2 B3 B4 B5 B6 B7 B8
FxTSx
RCLKx
SYNCHx
TIMING DETAILS

Figure 19.1 Timing for the I/O Data and Timing Connector

TABLE 19.1

37 POSITION I/O DATA AND TIMING CONNECTOR PIN ASSIGNMENT

Pin No.	Identifier	Description (See Note Pg 19.2)
1	B8ZS*	Low state when B8ZS code is detected
2	RPCM1	Recovered unipolar PCM from line 1
3	DGND	Digital Ground
4	RCK1	Recovered clock from line 1
5	D1D	Low state when D1D selection prevails
6	SYNC1*	Synch pulse associated with line 1 timing
7	N/C	No connection
8	F_TTS1*	Pulse coincident with F_T in line 1
9	SLC96*	Low state when SLC-96 selection prevails
10	RCK 2	Recovered clock from line 2
11	D5-ESF*	Low state when D5-ESF selection prevails
12	RPCM2	Recovered unipolar PCM from line 2
13	D3/D4/D5*	Low state when D3/D4/D5 selection prevails
14	DGND	Digital ground
15	EXT DL I	Input for external data link messages
16	EXT DL SEL*	Low state selects the external data link input
17	DLTS	Data link time slot or clock
18	D2*	Low state when D2 selection prevails
19	F_STS1*	Pulse coincident with F_S in line 1
20	FAULT1*	Low state when PCM or framing is lost on line 1
21	F_STS2*	Pulse coincident with F_S in line 2
22	FAULT2*	Low state when PCM or framing is lost on line 2
23	F_TTS2*	Pulse coincident with F_T in line 2
24	SYNC2*	Synch pulse associated with line 2 timing
25	ID	+5V/27 Ω
26	EXT CK I	External clock input
27	XFB1 TS	Pulse coincident with frame bit no. 1 in PCM output
28	STROBE 1	Pulse coincident with 8 bits of selected channel in line 1
29	RESET IN*	Low state input causes reset
30	STROBE 2	Pulse coincident with 8 bits of selected channel in line 2
31	N/C	
32	X STROBE	Pulse coincident with 8 bits of selected channel in PCM simulator 1
33	AUX IN SEL*	Low state selects auxiliary 64 kb/s input
34	DS0 DATA IN	64 kb/s data input
35	X CLOCK	PCM simulator 1 clock output
36	X PCM	Unipolar PCM signal delivered by the simulator 1
37	XFB TS*	Pulse coincident with frame bit in PCM output 1

Note: To ensure minimum pulse distortion and crosstalk, it is recommended to keep cabling length under 24" when connecting to the I/O Data and Timing Connector (J24). The use of flat ribbon cable is not recommended for cable length in excess of 12 inches.

9-PIN SIGNALING OUTPUTS CONNECTOR

19.3 This interface is marked J19 on the rear panel. It provides access to the signaling states associated with the selected channel on both DS-1 lines. This access is particularly useful when it is necessary to observe the timing relationship or precise duration of signaling/supervision signals with an oscilloscope or a strip chart recorder. The pin-out for this connector is given in figure 19.2. The description for each pin is given in table 19.2. Note: Pin number labels 1 and 5 on the 440B are reversed; figure 19.2 is correct.

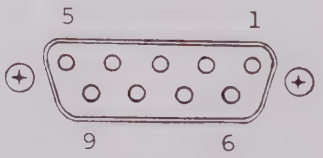


Figure 19.2 J19 Signaling pin-out

TABLE 19.2

9-PIN SIGNALING OUTPUTS CONNECTOR PIN ASSIGNMENT

Pin No.	Description
1	SIG A - Line 1
2	SIG B - Line 1
3	SIG C - Line 1
4	SIG D - Line 1
5	Ground

Pin No.	Description
6	SIG A - Line 2
7	SIG B - Line 2
8	SIG C - Line 2
9	SIG D - Line 2

With the exception of the ground terminal (5), all terminals exhibit three states. These states are defined as follows in terms of the corresponding signaling state display LEDs:

State	LED Color	Nominal Level w/o Load
1	red	+ 1.6 V
0	green	- 1.8 V
no op	OFF	0.0 V

The source impedance is 10,000 ohms for state 0 and 1; it is much larger than 10,000 ohms for "no op".

The "no op" state occurs when any of the following conditions is obtained:

- framing is lost on the line associated with the signaling bit
- the state is not legitimate for the format selected (i.e., SIG C or D when the system selection is not D5-ESF)

ACCESSORY

19.4 The 9-position connector, described in Section 19.3 and Table 19.2 can mate with 9-pin D-subminiature connectors provided by several manufacturers. In particular, AMP Inc. supplies the following connector components:

AMP P/N	Description
745032-1	HDJ-20 receptical housing
205311-9	HD-20 connector pin
207753-1	HDJ-20 plastic jacket
61831-1	Strain relief
91234-1	Insertion tool

T-COM can also supply a 4-foot, 9-lead cable assembly. This cable (T-COM P/N 2700-021) is terminated at one end by the AMP connector described above and is left unterminated at the other end to suit the application.

20. INSTALLATION

INTRODUCTION

20.1 This section contains a set of instructions for conducting the initial inspection of the newly received 440B, and for installing various accessories and options. Also included are repacking and shipping instructions.

INITIAL INSPECTION

20.2 Upon receipt of your new 440B, it is recommended to inspect the shipping container for damages. Should any damage be found, the container must be kept until all contents of the shipment have been checked for completeness and the instrument has been checked visually for mechanical integrity and electrically by verifying that the instrument satisfactorily complete the self-diagnostic routine described in chapter 3.

If the contents are incomplete or if there is mechanical damage or if the instrument does not pass the self-diagnostics routine, notify your T-COM sales representative.

If the shipping container is damaged, notify the carrier as well as the sales representative. Keep the shipping material for the carrier's inspection.

PREPARATION FOR RACK MOUNTING

20.3 When the 440B is to be installed in a relay rack, a rack-mounting ear must be secured to each vertical side of the instrument near the front panel as illustrated in figure 20.1 below. Each bracket is secured with two pan head 10-32 phillips screws. To install the 440B into a 19 inch wide rack use the bracket kit T-COM P/N 2750-032-P; for a 23 inch wide rack, use theT-COM P/N 2750-033-P.

If the 440B is equipped with option 52B or 53A, the same rack mounting brackets can be used.

FIELD INSTALLATION OF OPTIONS

20.4 All the options available for the 440B can be installed in the field by people having a minimal amount of mechanical skills. The procedures to be followed for installing options 03 through 07 are given in the following paragraphs. The procedures to be followed for installing options 52B and 53A are included in the instruction manual for these options. Only phillips type screw-drivers are required to complete the installation.

> **CAUTION**
> When carrying out any of the retrofitting procedures given below, the set must be disconnected from the AC power line. Failure to comply with this requirement can result in harm to the operator and/or the testset.

INSTALLING OPTION 03

20.4.1 The installation of option 03 consists in replacing a blank panel covering a rear panel opening by the optional DS0 interface unit. This unit consists of a printed circuit board equipped with a small metal case/panel securing jacks and connectors. The installation requires approximately 15 minutes and requires a phillips screwdriver suitable for #4 screws.

> **IMPORTANT NOTE:**
> The DS0 interface assembly capacitive adjustments (CT1 and CT2) are critical and one must be careful not to alter their settings. If a setting has been changed, refer to chapter *x* of this manual for calibration instructions.

To equip the 440B with the option 03, proceed as follows:

Step 1
Remove the six screws securing the rear panel to the bezel. Gently pry the panel loose from the bezel and let it rest horizontally on its four legs. Unplug the flat ribbon cable connecting the power supply board to the mother board by holding on firmly to the 20-position connector and by pulling vertically away from the mother board.

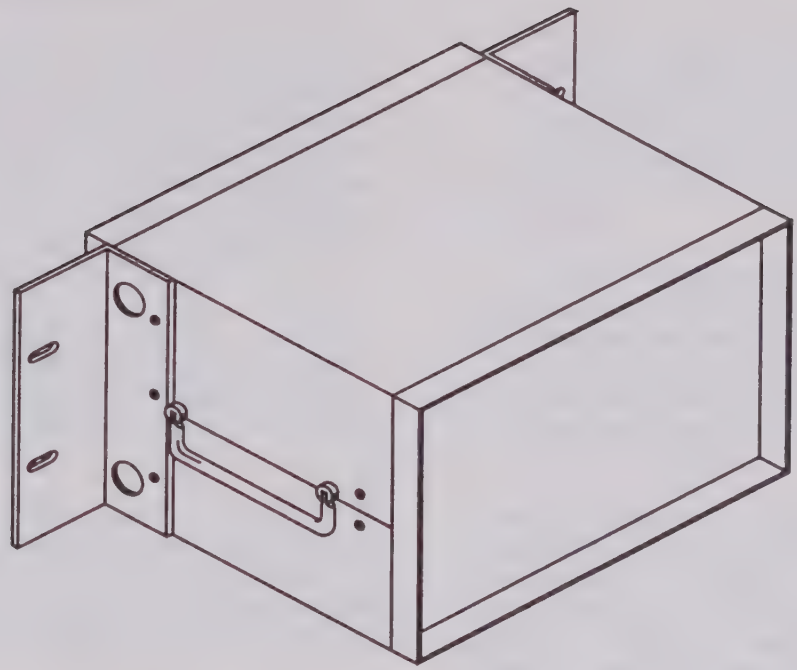


Figure 20-1. Mounting Bracket Installation

Step 2
Remove the four screws securing the blank panel to the test set rear panel and place the dummy panel aside. The dummy panel covers the cavity on the right side of the rear panel, and is of no further use once the DS0 option is installed.

Step 3
Unwrap the DS0 interface assembly and place it on the inside surface of the rear panel over the cavity previously covered by the blank panel. Secure the DS0 interface assembly to the rear panel with four screws. Do not over tighten.

Step 4
Place the rear panel horizontally on its legs and orient it in such a way that the power supply ribbon cable and the DS0 interface assembly ribbon cable are aligned respectively with their mating header on the mother board. Connect the two ribbon connectors to the corresponding male headers, making certain that they are properly aligned and fully engaged:

The power supply connects to J20.
The DS0 interface assembly connects to J27.

Note:
Alignment offset in either connector can result in substantial damage to the instrument.

Step 5
Gently fold back the rear panel into the normal resting position against the bezel and secure it in place with the six screws removed in Step 1.

This completes the DS0 assembly retrofitting procedure. Prior to placing the test set back into service, it recommended to verify that both the test set and the option perform properly.

This may be accomplished by supplying a 2047 pattern at 64 kb/s to the DS0 DATA input and to recover this pattern at the DS0 DATA output in an error free manner when the output PCM of Transmit 1 is patched to the PCM input of either DS1 Receiver.

INSTALLING OPTIONS 04, 07

20.4.2 The installation of options 04 and 07 is identical. It consists of replacing the Main MicroController board (MMC) in the 440B with one equipped with the appropriate option. To replace the MMC board, it is necessary to remove the top cover of the 440B or the add-on optional unit (52B or 53A) if one is installed. A separate step is included to address each case.

1a. Removing the top cover
The cover is held on by six phillips-head 6-32 screws, two on each side and two on the top. Remove these screws and lift the cover free of the chassis.

1b. Removing the add-on unit
Prior to attempting the removal of the add-on unit, it is required to remove the rear panel assembly of the instrument to gain access to the cables interconnecting the add-on unit to the mother board.

- The rear panel is secured to the instruments by six phillips-head 4-40 screws located along the periphery of the panel. Removed these screws and gently pull the panel away from the instrument. Detach the cable(s) connecting the rear panel assembly to the mother board of the instrument.

- The add-on unit is secured to the 440A by two phillips-head screws 6-32 on each side about half way up on the height of the instrument and one phillips head 6-32 screw near the middle of the rear panel of the add-on unit. Remove these screws and unsecure the cables connecting the add-on unit to the mother board by holding firmly on the cable connector and pulling vertically away from the mother board.

2. Replacing the MMC board
When the cover or the add-on unit is removed, refer to figure 20.2 to identify the MMC board. Gently nudge this board out of its slot by holding it along both vertical edges and exerting a vertical force directed away from the instrument.

The removed board should be set aside and the replacement MMC board pulled out from its protective packing material.

Install and seat the replacement board in the vacated slot with the component side facing the front panel. A force of several pounds must be exerted on the top of the board to insert it fully in the mating connector. As a precaution, check that the other boards are also well seated.

3. Completing the reassembly
Either the steps in 1a or 1b must be retraced to complete the reassembly process. Be sure to properly align each of the cable connectors with their mates on the mother board and to exert only moderate amount of torque when tightening the screws.

When the reassembly is complete, it is recommended to carry-out an operational check prior to returning the instrument to service, to ascertain that the installation is successful. To verify that the set operates correctly, it is simply necessary to power it up and to verify that the self-diagnostic routine is carried out to completion without eliciting any error message.

To verify that option 04 is operational, it is recommended to secure a suitable printer to the 440B RS-232-C port on the rear panel, and to configure the port following the instructions in chapter 17. The option 04 is operational if the downloading of data to the printer is performed as specified in that chapter.

To verify that option 07 is operational, it is recommended to follow the instructions given in chapter 15 of this manual.

INSTALLING OPTIONS 05, 06

20.4.3 The installation of options 05 and 06 is nearly identical. It consists of adding either the QRS board for option 05 or the Telephone No. board for option 06. To install these boards, it is necessary to first remove the 440B top cover or, if the 440B is equipped with an optional add-on unit, to remove this unit. To remove the top cover or the optional add-on unit, refer to the appropriate procedures in section 20.4.2. To install either option carry out the steps below.

- Installing the QRS board
This board is installed in the QRS slot illustrated in figure 20.2. To install the board, it must be inserted with components facing the front of the

instrument and guided to seat properly in the mating connector on the mother board. A force of several pounds must be exerted on the top of the board to insert it fully in the mating connector. As a precaution, check that the other boards are also well seated.

- Installing the Telephone No. board (TNB)

This board is installed in the TNB slot illustrated in figure 20.2. To install the board, it must be inserted with components facing the front of the instrument and guided to seat properly in the mating connector on the mother board. A force of several pounds must be exerted on the top of the board to insert it fully in the mating connector. As a precaution, check that the other boards are also well seated.

When the reassembly is complete, it is recommended to carry-out an operational check prior to returning the instrument to service, to ascertain that the installation is successful. To verify that the set operates correctly, it is simply necessary to power it up and to verify that the self-diagnostic routine is carried out to completion without eliciting any error message.

To verify that option 05 is operational, it is recommended to patch the Transmit 2 T1 output to the Receiver 2 PCM input and to select the DS1 #2 pattern 'framed QRS 2^{20}-1 w/14 0's max'. After having reset the instrument, the following observations should be made :

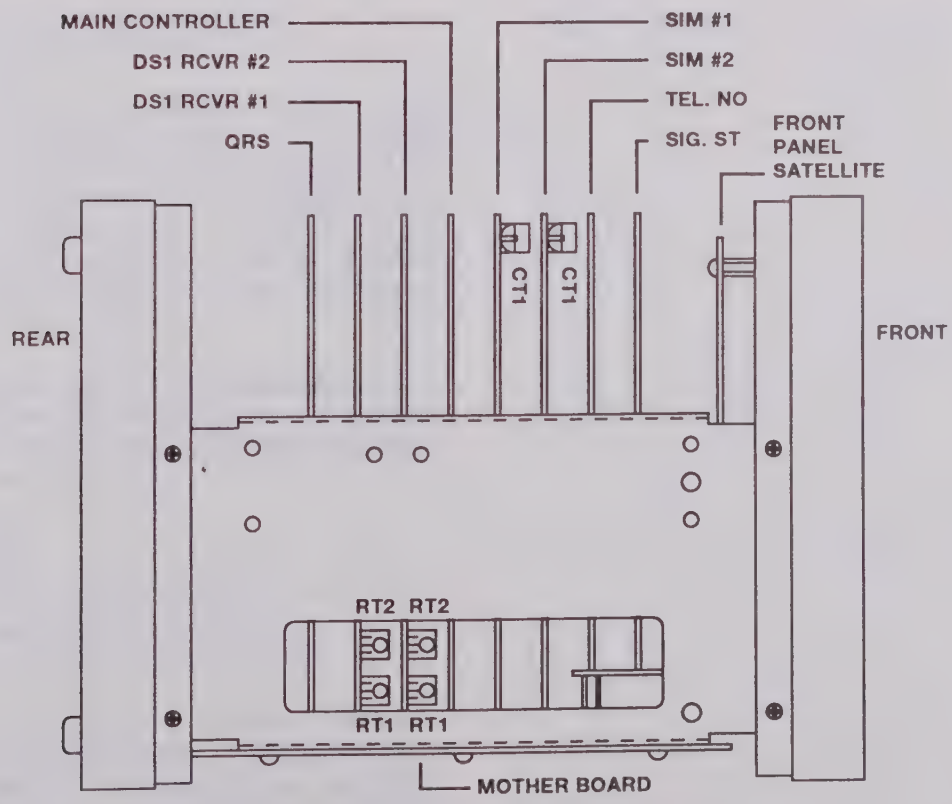


Figure 20-2. 440B PC board positions

- the SYNCH/BIT ERR LED in the DS1 Receiver 2 section is lit solid green
- all other LED's in the DS1 Receiver section are turned off
- the STATS/RCVR 2 bit error menu shows no activity. An example of this screen [1] is shown below.

Screen [1]

BIT ERR	SYNC L-SEC	BER
0	0	LOW ERROR PAT NXT

To verify that option 06 is operational, it is recommended to patch the Transmit 1 T1 output to the Receiver 1 PCM input and to observe that, when a DTMF encoded telephone number is sent, the same number is recovered and displayed by the VFDT. Refer to chapter *xx* for setting the transmitter to deliver the test DTMF encoded telephone No. and to chapter *8* for setting the DTMF telephone No. decoder.

REPACKING FOR SHIPMENT

20.5 The use of the original shipping carton and packing material is highly recommended. If the original packing material is not available, you may use any strong container. Wrap the instrument in heavy paper or a plastic bag and surround it with three or four inches of shock absorbing material to cushion it firmly and prevent movement inside the container.

Note: Your authorized T-COM representative is ready to assist you in any situation and you are always welcome to get directly in touch with the T-COM service department:

Customer Service:

T-COM
825 E. Middlefield Road
Mountain View, CA 94043
Tel: (415) 964-3415

All equipment returned to the factory must be accompanied by a manufacturer's Return Material Authorization number. In order to get an RMA number, customers should call in or write, with the model and serial numbers of equipment to be returned, PRIOR to shipment. A number will be issued, which will be referenced in both the packing slip and the purchase order associated with the equipment. Include with the instrument a comprehensive description of the problem(s) encountered to ensure that the instrument is satisfactorily repaired.

21. PRODUCT SPECIFICATIONS

* General
- System compatibility : DS1/D1D,D2, D3, D4, SLC-96TM, ESF
- Line format : T1/AMI & B8ZS

* DS1 Receiver (#1 or #2)
- Input frequency : 1.544 MHz +/- 1 kHz
- Input configurations : Terminated, bridging, monitor
- Input level range : 200 mV to 4 V base to peak
- Real time diagnostics : No PCM, BPV, CRC error, frame bit error, frame loss, all ones, AIS
- Channel selection : Any one of the 24 channels
- DS0/VF decoder
  - Frequency response : 300 Hz - 3000 Hz within .15 dB
  - Gain linearity : 0 to - 30 dBm0 = 0.25 dB
  - Quantizing noise : 0 to - 30 dBm0 = -33 dB
  - Idle noise : 13 dBrnC0 max
  - Output impedance : 600Ω+/- 1%
- DS0 Signaling decoder
  - Real time display : A, B, C & D bits w/ bi-color LED's
  - Real time output : On rear panel 9-pin connector

* Measurement Capabilities
- DS1 impairment statistics: DS1 input level & frequency slippage & frame slip count (0-9999 counts) BPV count, CRC error count, frame bit errors, errored-sec., severely errored-sec., consec. sev. errored sec., bit errors, frame loss-sec., frame bit error rate, CRC bit error rate.
- DS0 VF parameters
  - Level : +3.2 to -59.9 dBm0 / .1 dB accuracy
  - Noise
    - C-msg w/notch : + 10 to 93 dBrnC0 / 1 dB accuracy
    - C-msg : + 10 to 93 dBrnC0 / 1 dB accuracy
    - 4 KHz flat w/HP : + 10 to 93 dBrn0 / 1 dB accuracy
- DS0 Signaling : A, B, C, D bits for all 24 channels on both monitored lines are displayed simultaneously
- DS0 Data : Histogram representing the instantaneous 1/0 density for each bit in the selected channel. Identification of DDS 56 kb/s test patterns

* Speaker Amplifier
- Input : From DS1 Receiver 1, 2 or 1 & 2
- Gain : 0 to 40 dB, continuously adjustable
- Frequency response : 300 Hz - 3000 Hz within 3 dB
- Power : Up to 150 mW

* DS1 Transmit #1
- Operational modes : Stand alone or jointly w/Receiver #1 to provide drop/insert
- Internal Clock Rate : 1,544,000 +/- 30 Hz
- Pattern selection : Idle & 1005 Hz/-20 dBm0
- DS0 Tone Synthesizer
  - Level : +3.2 to -59.9 dBm0 by .1 db steps
  - Frequency : 50 to 3950 Hz by 10 Hz steps
  - Memory : Up to 16 discrete tones
- EXT VF Input/encoder
  - Frequency response : 300 Hz - 3000Hz within .15 dB
  - Gain linearity : to - 30 dBm0 = 0.25 dB
  - Quantizing noise : 0 to - 30 dBm0 = -33 dB
  - Idle noise : 18 dBrnC0 max
  - Input impedance : 600 Ω +/- 1%
- Signaling states : A, B, C, D settable to 0 or 1
- External sig. inputs : Contact closures or C-MOS
- Telephone Numbers : With option 06
- Internal DS0 data source : With option 05
- External DS0 data I/F : With option 03
- T1/PCM output : 3.0 Vpk +/- 10% in 100 Ω load

- MON/PCM output : 0.3 Vpk +/- 10% in 100 Ω load

- Miscellaneous
  - Yellow alarm : Not enabled in THRU mode
  - Data link access : 4 kb/s on ESF & SLC-96™ only

* DS1 Transmit #2
- Operational modes : Stand alone or jointly w/Receiver #2 to provide drop/insert
- Internal Clock Rate : 1,544,000 +/- 30 Hz
- Pattern selection : Idle & 1005 Hz/-20 dBm0
- EXT VF Input/encoder
  - Frequency response : 300 Hz - 3000Hz within .15 dB
  - Gain linearity : 0 to - 30 dBm0 = 0.25 dB
  - Quantizing noise : 0 to - 30 dBm0 = -33 dB
  - Idle noise : 18 dBrnC0 max
  - Input impedance : 600 Ω +/- 1%
- Signaling states : A, B, C, D settable to 0 or 1
- T1/PCM output : 3.0 Vpk +/- 10% on 100 Ω load
- Loop up/down : CSU, NI, up to 8 bit user defined
- Error injection type : BPV, frame bit, CRC or bit
- Error injection rate : Single or 5/sec

---

* QRS-Stress Pattern Sending & Receiving Capability (Option 05)

- DS1 SENDER
  - QRS patterns : Framed or unframed 2^{15}-1, 2^{20}-1 w/ 14 0's limit, 2^{20}-1, 2^{23}-1
  - Other patterns : Framed or unframed all ones, 1/8, 3/24 & user-selected 24 bit word

- DS1 RECEIVER
  - Real-time display : Bit error & pattern synchronization
  - Processed data : Bit error count, synch loss-sec., bit error rate (BER)

- DS0 SENDER
  - Pattern selection : 511, 2047, 8-bit user defined

- DS0 RECEIVER
  - Processed data : Errored-sec., block errors, synch loss-sec, bit error rate (BER)

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* Telephone No. Sending & Receiving Capability (Option 06)

- SENDER
  - Memory : Up to 16 telephone numbers
  - No of digits/char. : Up to 32 per phone No.

- MF & DTMF SENDER
  - Frequency accuracy : Within 1.5% of nominal
  - Level range : 0 to -30 dBm0 by steps of 1 dB
  - Level accuracy : +/- .2 dB
  - Digit duration : 30 - 99 ms by steps of 1 ms
  - Interdigit delay : 30 - 99 ms by steps of 1 ms

- DP SENDER
  - Repetition rate : 8 to 22 PPS by steps of 1 PPS
  - Percent Break : 30 to 80% by step of 1%
  - Interdigit delay : 100 to 990 ms by steps of 10 ms

- Receiver display : Up to 32 digits & characters

- MF & DTMF RECEIVER
  - Acceptance template : Per AT&T Notes on the Network
  - Rejection template : Same reference

- DP RECEIVER
  - Acceptance template : Per AT&T Notes on the Network
  - Rejection template : Same reference

- WINK MEASUREMENTS
  - No. of winks : Up to 3
  - Wink delay : Up to 999 ms
  - Wink duration : Up to 999 ms
  - Resolution : 1 ms

Accuracy : 5 ms

---

* DS0 data access interface (Option 03)

- Transmit input
  - Data : 64 kb/s unipolar, TTL level
  - Supplied timing : balanced 8 and 64 kHz clocks
  - Compatibility : KS 20909/TPI 109A
- Receive output
  - Data : 64 kb/s unipolar, TTL level
  - Supplied timing : balanced 8 and 64 khz clocks
  - Compatibility : KS 20908/TPI 108A
- XMT/RCV Timing : Synchronized or independent to operate with TPI 108/9 RT

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* RS-232-C printer port interface (Option 04)

- Transmission type : Full duplex
- Transmission format
  - Character set : ASCII, 8 bit
  - Baud rate : 300 - 9600 selectable
- Electrical interface : Standard DB-25 female connector
- Compatibility : RS-232-C (DTE)

---

* Miscellaneous Capabilities

- Real time clock and calendar for impairment event stamping
- Elapsed test timer (00:00:00 to 99:59:59)
- Selectable beeper (on/off) function
- Context sensitive HELP screens
- 37 pin connector providing access to timing signals (for attachment of future add-on units)
- Compatibility with : 53A DS1C/DS1 Monitor/Demux and 52B DS3/DS2/DS1 Monitor/Demux

* Other Features and Capabilities

- Real-time clock and calendar for impairment event stamping
- Elapsed test timer
- Selectable beeper (on/off) function
- Context-sensitive HELP screens
- 37-pin connector providing access to timing signals (for attachment of future add-on units)
- Compatibility with 53A DS1C/DS1 Monitor/Demux and with 52B DS3/DS2/DS1 Monitor/Demux options

* Miscellaneous

- Front panel jacks : Long frame bantam
- Message display system: Two rows of 40 characters, vacuum fluorescent tube
- Powering requirements: 108 to 126 VAC, 60 Hz, 16 W nom.
- Operating temperature: +5 to + 45°C
- Storage temperature : -40 to 70°C
- Humidity : Up to 90% non-condensing
- Dimensions : 8.5" x 11.5" x 13.5" (HxDxW)
- Weight : 21 lbs w/options 03, 04, 05, 06 and including protective front cover

* Notes

- ™ SLC-96 is a trademark of AT&T Technologies
- Specifications are subject to change without notice.

22. SELF-TESTING PROCEDURES

This chapter is in preparation. It will be included in the next release of this manual and sent to those persons from whom we have the warranty registration card on file.

23. FIELD MAINTENANCE AND CALIBRATION

This chapter is in preparation. It will be included in the next release of this manual and sent to those persons from whom we have the warranty registration card on file.

Description

4140E Instruction Manual
Fuse 3/8A SB
6-ft. 3-conductor power cord
Front cover assembly for 4140B only
Front cover assembly for 4140B
with 52B or 53A

24. ACCESSORIES AND REPLACEABLE PARTS

Accessories	Description
2888-001	Canvas Carrying Case (440B only)
2888-003	Canvas Carrying Case (440B equipped with 52B or 53A option)
2887-002	Hardshell Case with Padding (440B only)
2887-004	Hardshell Case with Padding (440B equipped with 52B or 53A option)
2750-032-P	19 inch Rack Mounting Kit
2750-033-P	23 inch Rack Mounting Kit
1470-001	Printing Terminal TI model 703
2902-440-B0	Training Video Tape (VHS format)

Cables	Description
1700-031	6-Ft Male/Male RS-232-C Cable
2700-032	6-Ft Male/Male RS-232-C Cable with null modem configuration
2700-034	6-Ft Male/Male RS-232-C Cable with null modem configuration for TI 743
2700-021	9-Lead Signaling cable assembly
1690-001	4 Ft Patchcord with bantam plugs
1690-002	4 Ft. Patchcord with bantam & 310 plugs
1690-003	8 Ft. Patchcord with bantam plugs
1690-004	8 Ft. Patchcord with bantam & 310 plugs
1690-005	2 Ft., 75 Ohm patchcord with miniature (WECO 440)plugs
1690-006	4 Ft, 75 Ohm coaxial patchcord with standard (WECO 358) patch plug and male BNC plug
1690-007	4 Ft, 75 Ohm coaxial patchcord with standard (WECO 358) patch plugs
1690-008	2 Ft, 75 Ohm coaxial patchcord with standard (WECO 358) patch plug and male BNC plug

Adapters	Description
1694-001	Bantam-to-310 adapter plug
1694-002	Standard (WECO 358) patch plug /BNC female adapter
1694-003	Mini (WECO 440)patch plug /BNC female adapter
1694-004	100 Ohm termination plug - 310
1694-005	100 Ohm termination plug - Bantam

Replaceable Parts	Description
IM440B01	440B Instruction Manual
1500-004	Fuse 3/8A SB
2700-013	6-ft, 3-conductor power cord
2751-076	Front cover assembly for 440B only
2751-077	Front cover assembly for 440B with 52B or 53A

Notes:

- With the exception of transportation costs, there is no charge for repair of instruments under warranty.

- Estimates of charges for non-warranty or other service work will always be supplied, if requested, before work begins.

25. WARRANTY

T-COM products are warranted against defects in materials and workmanship for one year from the date of shipment. Our obligation is limited to repairing and replacing products that prove to be defective during the warranty period as a result of normal and intended use of the product. This warranty does not apply to defects resulting from misuse, negligence, accidents or unauthorized repairs or modifications.

T-COM does not assume any liability for consequential damages. We reserve the right to make changes in design and construction of our products at any time without incurring any obligation to alter units previously sold.

This warranty is in lieu of any other warranty expressed or implied except as specifically modified in writing by an officer of T-COM.

Notes:

- With the exception of transportation costs, there is no charge for repair of instruments under warranty.
- Estimates of charges for non-warranty or other service work will always be supplied, if requested, before work begins.

RECEIVED

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Packing Slip #: S-03779

From: *T-COM Corporation*
825 East Middlefield Road
Mountain View, CA 94043-4080
(415) 964-3415

Ship To: GTE North Inc
General Supply Center
RFD#3 Route 9 West Bldg#3
Bloomington, IL 61704
ATTN:

Bill To: GTE North Inc
PO Box 90246
San Angelo, TX 76902-0246
ATTN: Accounts Payable--IL Opns

Cust PO: S 0164709	SO#: 901017-02	Ship Date: 5-Dec-90
SLS: RM	Rep:	CN INV#:
Shipped Via: UPS	Terms: Net 30	RMA#:

Item #	Qty Ord	Qty Shpd	Qty B.O.	Part Number/Description
1	1	1	0	T-COM Model [SPECIAL]4408 Digital Communications Test Set. Serial# 0438 .
	1	1	0	Opt 03 Send & Receive DSO Interface
	1	1	0	Opt 04 Terminal/Modem RS-232-C Port
	1	1	0	Opt 05 ORSS/PRSS
	1	1	0	Opt 06 MF/DTMF/EF Telephone No.

LL Bow
R. Tomlin

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DEC 11 1990

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ACCOUNTS ARE DUE & PAYABLE ACCORDING TO THE TERMS STATED ABOVE.
1.5% INTEREST PER MONTH WILL BE CHARGED ON ALL PAST DUE ACCOUNTS.

fuse holder) as shown figure 6.1 below. This jumper has a length of approximately one inch and can be made with AWG #24 or larger plastic insulated copper wire. The above procedure should be skipped for the version 52B-1 as it does not have a power relay.

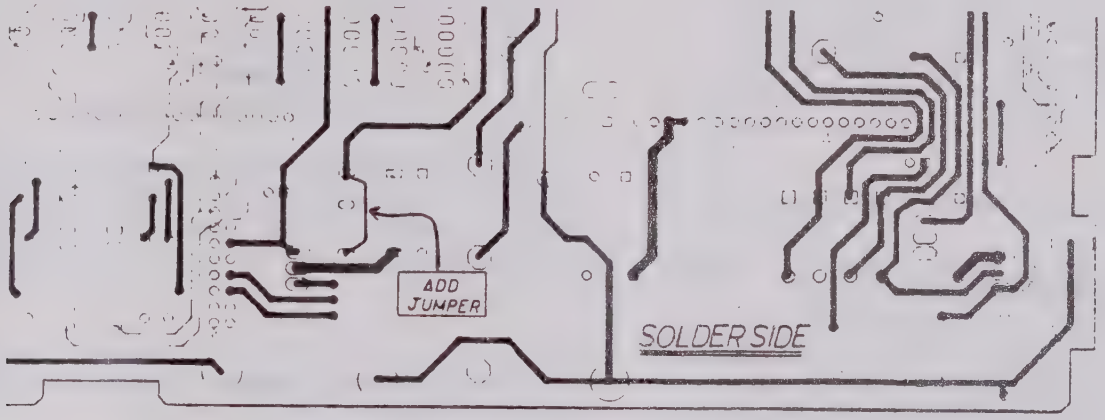

Fig 6.1 Shorting K3 relay contacts

To ensure that no short circuits result when the assembly is under power, the two boards must be resting on an insulated surface. When handling the 52B bottom board assembly, care should be paid to avoid repeated bending of the 3 flat ribbon cables; this precaution will avoid breakage of these cables.

Similarly, it is a sound precaution to minimize wear on the two ribbon cables interconnecting the top and the bottom assemblies. At this point, the assembly is ready to be powered-up.

> **CAUTION**
>
> While AC power is applied to the assembly, 115VAC is present on the area surrounding the large power transformer. Care must be taken to avoid electrical contact with any circuit in this area as dangerous, potentially lethal, shock can result.

Powering is accomplished by connecting an AC power cord between the AC inlet on the lower board assembly and the 115VAC power line.

Generic name	Recommended set
DS3 pattern generator	Tau-tron S5200D transmitter
10 MHz frequency counter	HP 5314A
DVM or DC voltmeter	any
Oscilloscope 100 MHz bw	Phillips PM3267
Low cap 10X probe	Tektronix P6202A

Table 6.1
Required test instruments

- Required test instruments

6.3.3 A list of the test instruments required to perform the calibration is given above in table 6.1. Any instrument with equivalent capabilities can be substituted.

- Power supply operational check

6.3.4 Prior to performing the calibration proper, it is desirable to verify that the power supply voltages and ripple levels are within specifications. Refer to table 6.2 for acceptable range of values applicable to the supply voltages. When testing for level and 60 Hz ripple, the instrument return lead must be grounded. The heat sink on which the AC inlet is secured can be used as ground.

Connector /Pin	Voltage Range	Ripple (mV pk-pk)
P1/4	4.80 to 5.20	50 max (60 Hz)
P1/3	-4.80 to -5.20	50 max (60 Hz)
P1/1	11.50 to 12.50	50 max (60 Hz)

Table 6.2
Power supply requirements

With an oscilloscope connected as listed in table 6.2, verify that the peak to peak ripple is within the tolerance listed for each voltage. Ignore the high frequency noise, only the 60 Hz component is important here.

- DS3 Front-end operational check/calibration

6.3.5 The DS3 front-end calibration requires the patching of one of the six S5200D DS3 outputs directly to the 52B top assembly DS3 input.

1. Set the S5200D controls as follows :
   - Power : on
   - Error mode : Error free
   - Frame : DS3-Frame
   - Pattern : 1111 [this requires that one of the rear panel switches be set to 1111]
   - Level : DSX
2. Set the 52B bottom PCB assembly INPUT SEL to TERM and power the assembly.

The calibration of the DS3 clock recovery circuit requires the adjustment of CT1. This air capacitor trimmer is located near the DS3 input jack; its adjustment requires a small size blade screw driver and to follow the next few steps :

- connect the scope probe tip to TP10.
- connect the scope probe ground to the ground TP located near TP3.
- adjust CT1 to obtain the maximum amplitude of the sinewave (approximately 250 mV pk-pk)

Remark

When the clock circuit calibration has been completed, all LED's in the DS3 DIAGNOSTICS section should be turned off and only the FR LOSS LED and the AIS LED in the DS2 DIAGNOSTICS section must be lit. If this is not the case, troubleshooting of the assembly by the factory is called for.

- DS1 Front-end operational check/calibration

6.3.6 The calibration of the DS1 clock recovery circuit requires the adjustment of CT3. In the unlikely event that CT3 cannot be adjusted properly, C48 (located near the small shield on the top board) may have to be selected to place CT3 near the middle of its adjustment range when the clock is properly calibrated.

With the DVM connected at TP7, adjust CT3 to read 2.6 to 2.8 VDC. If the rotor blades of CT3 are engaged from a third to two thirds or the way in, the adjustment is satisfactory. If not, it may be necessary to select a different value for C48. If changing C48, be sure to use a capacitor with an NP0 temperature coefficient.

To determine the appropriate value for C48, proceed as follows :

- connect the counter probe to monitor pin 2 of the IC located at the intersection of labels 5 and F on the edges of the top board
- select the value of C48 that brings the counter to read 1.544 MHz within 5 KHz and, with power off, solder this cap in place.

- Final steps

6.3.7 With CT1 and CT3 adjusted, the calibration is now complete. The PC board assembly should be reinstalled in the enclosure. To carry out the reassembly process, it may be convenient to follow the procedure given in paragraph 6.3.1 in reverse order. Because it is much easier to install the front panel while the bezel is in place, it is recommended to separate the front panel from the bezel prior to reassembly. This is accomplished by removing the four phillips screws securing the front panel to the bezel.

Remark

When the clock circuit calibration has been completed, all LED's in the DS3 DIAGNOSTICS section should be turned off and only the FR LOSS LED and the AIS LED in the DS2 DIAGNOSTICS section must be lit. If this is not the case, troubleshooting of the assembly by the factory is called for.

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MA27733